Faculty Profile

Name of Faculty	Prabhavathi P	
Department	Electronics and Communication Engineering	
Qualification	M.Sc.(IT), M. Tech. (Ph. D)	
Designation	Associate Professor	
Area of specialization	VLSI Design	
Date of Joining BNMIT	01.08.2005	
Nature of Association (Regular/Contractual/Adjunct)	Regular	
e-mail	prabhavathip@bnmit.in, prabha1010@gmail.com	
No. of years of Experience	Teaching: 24 years	

Academic Qualifications

- **Pursuing Ph. D** under the guidance of Dr. Veena S. Chakravarthi (Status: Course work completed)
- **M.Tech.** (2011), UTL Technologies Pvt. Ltd, VTU Extension PG Centre, VTU.
- **M.Sc.(IT)** (2005), Karnataka state Open University.
- **B.E.** (1988), JNNCE, Shimoga, Mysore University (I Class).

Working Experience Details

- Associate Professor, Department of ECE, BNMIT, Bengaluru since 2012
- Lecturer, Department of ECE, BNMIT, Bengaluru, since July 2005
- HoD, Department of Electronics, The National College, Basavanagudi, Bengaluru(Dec. 1998 to June 2005)
- Lecturer, SJR College for Women, Bengaluru (July 1994 to Nov.1998)
- Lecturer, DVS Polytechnic, Shimoga (Dec. 1989 to April 1990)
- Lecturer, BIET, Davanagere, Karnataka(Aug. 1989 to Nov. 1989)

Subjects taught

Analog Electronic Circuits, Electronic Communication, Wireless Communication, Fundamentals of CMOS, HDLs, ASIC Design, Analog VLSI Design, Low Power VLSI Design, RF CMOS Design

Research Experience Details:

Research ProjectsCompleted

Title: ***Design of load aware adaptive drive strength CMOS Standard cell library***
Funding Agency: VTU, Belgaum, Karnataka, INDIA
Amount: 10 Lakhs
Duration: 03 years (July 2011 – July 2014)
Principal Investigator: Dr. Veena S. Chakravarthi
Co – Investigator: Prabhavathi P
Status: Completed

Academic Positions and other Responsibilities (Institute Level):

1. **Coordinator**, FDP on Physical Design Challenges in DSM node VLSI Systems – January 2017
2. **Speaker for the session on SDC commands in Physical design in** FDP on Physical Design Challenges in DSM node VLSI Systems – January 2017
3. **Invited talk at Acharya Institute of Technology on Physical Design Challenges** in FDP on Physical design using Innovus – July 2019

Experimental/ Computational/ Any other Skills:

A. IP Design

- **Eight**different IP s (Protocolbased and RTL proven) have been designed which can be fabricated or utilized in other designs.

B. Analog Design

- **Compressive Sensing in 180 nm**
- **Low Dropout Regulator in 90 nm and 45nm.**
- **SAR based 7 bit ADC**
- **K Delta 1 Sigma ADC(8 bit) with 56db SNR**

Instruments Handled/Software's handled:

- **Digital design using Cadence CAD tools – ncsim, RC, Innovus, Voltus, Conformal, (Behavioral to Physical design)**
- **Analog Design using Cadence CAD tools – Schematic editor, Layout editor, Hierarchy editor (Schematic to Physical Design)**

Awards/ Achievements/Memberships:

- Best design award for SAR based 7 bit ADC, NMIT, Bengaluru.
- Best paper award for "Coding data for energymiser wireless sensor network for data acquisition systems", VIT, Bengaluru.

Professional Memberships:

- **Life Member, Indian Society for Technical Education (ISTE).**
- **Life Member, Karnataka Rajya VijnanaParishath (KRVP)**

Research Publications:

I. In National & International Journals

International Journals:

1. Rekha P, Prabhavathi P, Veena S. Murthy, Padmaja Jain **"A Survey of Floral Aroma Sensors"** published in International Research Journal of Engineering and Technology (IRJET) e-ISSN: 2395-0056 Volume: 05 Issue: 07 | July 2018 www.irjet.net, p-ISSN: 2395-0072

2. Prabhavathi P, Nikhita V "**Design of Low-Dropout Regulator" published In** International Journal of Applied Research, Volume 1, Issue 7, Page no. 323-330, 2015
3. Prabhavathi P, Namratha N Petkar, "Implementation of 5 Bit Error Correcting BCH IP Core of Code length 255 on FPGA" Published in IJERM Volume 03 Issue 07 (July 2016)

II. In National/International Conference Proceedings

1. Prabhavathi P, Amulya Rao, Vandana Rao, Rachana Ramkumar "Compressive sensing using 180 nm Technology" in 4th International Conference on recent trends in Electronics, Informatics, Communication and Technology -2019 (RTEICT) at SVCE, Bengaluru, India – 17th -18thMay 2019.
2. Prabhavathi P, Anuragini K "IOT based lightning prediction system and measurement of different weather parameters" in International conference on Multimedia Processing, Communication and Information Technology MPCIJ 2019 at JNNCE, Shivamogga, Karnataka during 8 -9, June 2018.
3. Prabhavathi P, Asha S "Novel Communication Interface for IoT Applications" at 30TH INTERNATIONAL CONFERENCE ON VLSI DESIGN & 16TH INTERNATIONAL CONFERENCE ON EMBEDDED SYSTEMS. 7th -11thJanuary 2017 Hyderabad, India.
4. Nagendra P. B, Prabhavathi P, Namratha N Petkar, "Implementation of 5 Bit Error Correcting BCH IP Core of Codelength 255 on FPGA" in National Workshop on Cryptology NWC – 2016,11th -13th , Aug.2016, organized by Jawaharlal Nehru National College of Engineering Shivamogga, Karnataka
5. Prabhavathi P and Nikitha V "Design of Low- Dropout Regulator"published in International Journal of Applied Research, Volume 1, Issue 7, 2015, page no. 323 – 330.
6. Prabhavathi P, Mahesh N B, Subodh Kumar Panda "Design of A 12-Bit Cyclic Vernier Ring Time-to-Digital Converter"at VCASAN -2013- International conference on VLSI, Communication, Advanced Devices, Signals & Systems and Networking, BNMIT, Bangalore, July 17-19, 2013
7. Manu B N, PrabhavathiP "Design and Implementation of AMBA ASB APB Bridge for ARM SOCs", at Student Conference of VCASAN -2013- International conference on VLSI, Communication, Advanced Devices, Signals & Systems and Networking, BNMIT, Bangalore, July 17-19, 2013
8. Pournima P R, PrabhavathiP,"Design of Rail-to-Rail op-amp in 90 nm CMOS"at Student Conference of VCASAN -2013- International conference on VLSI, Communication, Advanced Devices, Signals & Systems and Networking, BNMIT, Bangalore, July 17-19, 2013
9. Shwetha H N, Prabhavathi P "7 bit, 200 KSPS SAR ADC with Ultra low energy DAC and Clocked Comparator"at National Conference NCCSC – 2012 at KSIT, Bangalore, August 6, 2012(Adjudged best paper & presentation).
10. Veena S K, Prabhavathi P "Low Latency Parallel Architecture DPLL", at National Conference National conference on VLSI and Communication System(VCS), at BIT, Bangalore, 30 & 31st October 2012.
11. Ramya Rajan, PrabhavathiP ,Dr. Veena S Chakravarthi,"Design of a 4 bit accumulator using new 45nm low leaky standard cells", IP-SoC 2011 Conference, Grenoble, France, Dec 7-8, 2011.
12. Ramya Rajan, Prabhavathi P,Dr. Veena S Chakravarthi,"Study of effectiveness of circuit level leakage power optimization techniques in DSM CMOS cells" at Proceedings of the International conference on Energy & Electrical systems ICEES- 2011, Kualalumper, Malasia.
13. Prabhavathi P, Dr. S B BhanuPrashanth, Premananda P "Modeling and Design of K Delta 1 Sigma ADC" at NCSCV10, SDMCET,Dharwad, Aug 13th 2010.
14. Prabhavathi P, Dr. S B Bhanu Prashanth, Premananda P"Design of K Delta 1 Sigma ADC" at NEWS10, BMSCE, Bangalore-04, Aug 4th 2010.

15. Prabhavathi P, and Dr.Veena S.Chakravarthi"At speed scan test challenges and future scope of work – A Survey", National conference on Recent trends in Instrumentation, Communication and Microelectronics INCOMM – 10, April 9th and 10th 2010 at ShriVaishnav Institute of Technology & Science, Indore(MP). (Adjudged best in faculty category).
16. Prabhavathi P, Dr. M. S. Suresh"Coding data for energy miser wireless sensor network for data acquisition systems", Prabhavathi P; National level conference on "Modern Trends in Communication" Oct 15-16, 2008; Vemana Institute of Technology, Bangalore. (adjudged best in category).
17. Prabhavathi P "A Study of Substrate technology and survey of modeling techniques for substrate resistance extraction" Paper presented at the National Conference on Next Generation Networks at B N M Institute of Technology, Bangalore in March 2007.

Conferences Attended

1. VCASAN-2013, BNMIT, Bangalore 17-19 June 2013
2. VLSID 2013 At Pune, India on Fellowship from 7th Jan to 9th Jan 2013
3. VDAT 2014 at P S G Tech, Coimbatore on Fellowship from 16th to 18th July 2014
4. VLSID 2014 at IIT-B, Mumbai from 5th to 7th Jan 2014
5. VLSID 2017 at Hyderabad 5th – 7th Jan 2017

Participation in Training courses/Seminars/Workshops

1. Attended FDP at NIT Calicut and **"CMOS Design"**(24th -30th June 2013).
2. Attended Didactic workshop on " **Electronics System Design , Manufacturing & Testing (ESDMT)**" (27thJuly – 31st July 2015).
3. Attended FDP on **"Micro and Nano Sensors for Health Monitoring"**at MSRIT Bengaluru, from 6th to 11th June 2016(Supported by TEQIP –II and IEEE Sensor Council/Bangalore Section).
4. Attended FDP on **"Computer and Wireless Networks"**Department of ECE, BNMIT, held between 11th to 16thJuly 2016.
5. Attended six days FDP on **"Physical Design challenges in DSM Node VLSI systems",**16thto 21stJanuary 2017at BNMIT, Bengaluru.
6. Attended FDP on **"Artificial Intelligence and Machine Learning"** by Cognizant in BNMIT, 20th and 21st June 2019.
7. Attended FDP on **" IOT based Project Design and Development" from** 24th to 29th June 2019 at Department of ECE, BNMIT, Bengaluru

Visits Abroad:

1. Visited Grenoble, France in December 2011 to present a design "**Design of a 4 bit accumulator using new 45nm low leaky standard cells**" at IPSoC,

Personal Details:

- **Date of Birth:** 25 - 04 –1967
- **Gender**: Female
- **Marital Status:** Married with two daughters

31st August 2018 **Prabhavathi P**