Faculty Profile

Name of Faculty	**Dr. Veena S Chakravarthi**
Department	Electronics and Communication Engineering
Qualification	BE, M.Tech, Ph.D
Designation	Professor
Area of specialization	VLSI Design, Networking, Communication Systems, Sensor Networks, Bio Medical Systems.
Date of Joining BNMIT	19/02/2010
Nature of Association	Head, Research, Adjunct Professor, ECE Department
e-mail	veenasc@bnmit.in; scveena@gmail.com
No. of years of Experience	25 years of Industry 5 years of Teaching and Research

Academic Qualifications:

- **Ph.D.** (2008), Department of Electronics and Communication Engineering, Bangalore University, India.
- **MPT** (1995), IIM, Bangalore, 9 Months residential management program equivalent to PGDM.
- **M.Tech.** (1991), Electronics Engineering, B M S College Of Engineering, Bangalore University, India.
- **B.E.** (1986), S D M College of Engineering, Dharwad, Karnataka University, Karnataka, India.

Working Experience Details:

- Research head for BNM Institution of technology, Bangalore since March 2019 till date
- **Technical Consultant,** Prodigy technovation, Bangalore Jan 2019-till date.
- **Consultant,** Prithvi 3 chip design, Digital TV Broadcast Technology ATSE 3.0, Saankhya Labs, Bangalore Jan 2018-May 2018.
- **Co Founder and CTO**, Healthcare Sensesemi Technologies Pvt. Ltd April 2015- Till Date.
- **Expert Consultant,** Wireless Technologies, Asarva Chips and Technology, April 2017- Till Date.
- **Vice President**, Digital Omniband Core, Asarva Chips and Technology, April 2015- March 2017.
- **Director-Engineering**, MAC Core, Asarva Chips and Technology January 2015- March 2015.
- **Professor*,** Department of ECE BNM Institute of Technology, *EPON consultant for Ikanos Technologies Pvt. Ltd, *Technology consultant for Parera Ventures, *System architect and expert consultant Asarva chips and Technologies, Feb2010 –Dec2015.
- **Senior Manager,** Optical Group Transwitch India Pvt. Ltd. July2009- Jan2010.
- **Senior Manager,** Optical Group Centillium India, July 2004- July2009.
- **Manager**, Optical Group Centillium India, Jan 2004 – June 2004.
- **Sr. Staff Engineer**, Optical Group Centillium India June 2003-Dec 2004.
- **Technical Manager**, Hardware Group, Mindtree Consulting Pvt. Ltd., Bangalore. 2000-2003.
- **Senior Engineer,** Microelectronics Division ITI Limited, 1995 – 2000.
- **Executive Engineer,** Microelectronics Division ITI Limited 1991 -1995.
- **Asst. Executive Engineer,** Microelectronics Division ITI Limited 1987- 1991.

Subjects taught:

CMOS VLSI Design, Analog mixed mode VLSI Design, SoC Design, Advances in VLSI Design, HDL Programming. VLSI Design and Verification, Low Power VLSI Design.

Research Experience Details:

1. Awarded research grant of Rs. 17 Lakhs from VTU-VGST on **"Adoptive load aware standard cell development"** 2011-2013
2. PhD for the work on **"Generalized Power Optimization Methodology for Application Specific Integrated Circuits (GPOM),** from Bangalore University 2008. A number of systematic investigations have been carried out to define GPOM. ASICs/SoCs with low power consumption can be developed by adopting GPOM methodology. GPOM describes the relevant techniques for power optimization at different stages of logic design till the timing closure stage of the ASIC design. CoolSoC technique which remaps the standard cells of high drive strengths to just enough drive strengths from the library in the design netlist guarantees low power if library contains multi drive strengths.

Patents:

1. Inventor in US Patent: **"Smart wearable device for health watch"** for Sensesemi Technologies Pvt. Ltd., Bangalore; US-PTO: 10,194,862
2. Inventor in India Patent pending for Patent Pending **"Smart wearable device for health watch"** for Sensesemi Technologies Pvt. Ltd., Bangalore;
3. Inventor in India with patent no: 201641022110: **"Method, System and Apparatus for Asynchronous SoC Testing and Validation"** for BNMIT, Bangalore

Professional Highlights:

1. Setting up ATE production testing department of Hybrid microcircuits and ICs at ITI ltd., Bangalore. Selected for deputation to pursue 9 months residential course on Management program for Technologists at IIM Bangalore.
2. Being a second member of the hardware team at Mindtree Consulting involved in growing up hardware team to 35 member team and design infrastructure in two years.
3. Technical lead for Bluetooth baseband core development and qualification at Mindtree. Supported marketing to win major orders on Bluetooth core.
4. Technical Lead for design of the WLAN IP core development at Mindtree which is included in their MINT IP portfolio.
5. Recipient of Mindtree chairman's award for the contribution in MINT program
6. Designed a MPCP block in EPON CPE SoC at Centillium India Pvt. Ltd.,Bangalore
7. Managed next generation EPON CPE SoC development, characterization, productionisation and validation support.
8. I was responsible for IC front design and physical design interface, characterization and productionisation of the ICs, their validation in Centillium as Senior Manager of IC Engineering (except analog and full custom which is done at a different site). This job requires me to be responsible for development of devices, interface with other functional groups like SW, validation and board development teams, ATE & production teams, yield improvement activities, external agencies like tool & IP vendors, fabs, package design groups customers etc.

9. Six multimillion SoC tape outs and around 20 IP core designs to my credit.
10. I was PON consultant to Ikanos Communications and Pereira Ventures for the development of PON products.
11. Incubated Asarva chips and technologies in the BNM campus and initiated WLAN SOC digital design. The company grew to 100 employees and taped out 60 Ghz radio test chip in one year. Asarva chips and technology was awarded best product startup and Best technology startup by silicon India group for two successive years till last year. Closely worked with its CEO for fund raising.
12. Architected Tri band WLAN SOC digital block based in IEEE 802.11ad, ac and Legacy standards.
13. Guided one research scholar towards her PhD on asynchronous DFT test methodology and filed a patent on JTAG based Asynchronous Scan testing
14. As Co-Founder and CTO, defined the technical requirement and Roadmap for healthcare device in Sensesemi technologies Pvt. Ltd.
15. Incubated Sensesemi Technologies research lab at BNM Institute of technology, Bangalore.
16. Currently technical consultant for Prodigy technovation pvt. ltd., Bangalore

Important Projects Handled:

1. Test generation and production testing of ICs used in PCM, E10B exchanges and DRDO projects. IP Core designs for ANURAG project of DRDO at ITI ltd.,
2. Bluetooth Base band IP core development at Mindtree consulting Pvt. Ltd.
3. WLAN MAC core IP development and validation at Mindtree consulting Pvt. Ltd.
4. MPCP block development in EPON CPE chip
5. Managed complete next generation EPON CPE SoC design, DFT support, support for SW interface, Validation and product ionization of CPE SoC.
6. Managed VoIP and Router SoC front end design.
7. Managed FPGA project for VoIP and Router SoC data path porting for early validation.
8. Managed Optical Gateway MCM product definition and development
9. Managed distributed development of next generation Voice enabled optical CPE chip jointly developed by Transwitch and a Chinese design centre.
10. Incubated a startup Asarva chips and Technology at BNMIT campus and managed design center for WLAN SOC digital design
11. Taught Low power VLSI, advanced SOC design subjects to Graduate students
12. Recipient of 17Lakh INR grant for research on low power standard cell development from Visvesvaraya Technological University during academic career.
13. SoC Processor selection and defining UPF Design Flow guidance and review for low power architecture for ATSE 3.0 SOC.

Work Experience Details in Industry:

As a part of Industry experience managed following activities:

1. Test generation and production testing of ICs used in PCM, E10B exchanges and DRDO projects.
2. VLSI designs for ANURAG project of DRDO at ITI ltd.,
3. Bluetooth Baseband IP and Wireless LAN (WLAN) MAC core development at Mindtree consulting Pvt. Ltd.
4. Managed complete next generation EPON CPE SoC design, DFT support, support for SW interface, Validation and productionization of CPE SoC in Optical domain.

5. Managed VoIP and Router SoC front end design in networking domain.
6. Managed Optical Gateway MCM product definition and development
7. Managed distributed development of NG Voice enabled CPE chip by Transwitch & Chinese design center.
8. Incubated Asarva chips and Technology at BNMIT campus and initiated WLAN SOC digital design
9. System Architecture definition for IEEE 802.11ad, ac and legacy WLAN Omniband SOC
10. Worked actively with the CEO for fundraising for the company.
11. Indian Patent filed on Asynchronous DFT Scan Testing
12. Designed Mems based blood pressure sensor and project was accepted for fabrication by INUP program, IISc but could not proceed on that due to other industry assignments.
13. Senior Member, IEEE and Chairperson IEEE Nano Tech council, Bangalore section and the IEEE Senior Member.
14. Reviewer in IEEE for VLSI Training modules for their E-blending Program.
15. Organized International conference on VLSI, Communication, Advanced devices, Signals & Systems and Communication VCASAN 2013 in July 17-19'2013; Editor, Proceedings of VCASAN 2013 published by SPRINGER.

Awards/ Achievements/Memberships:

- Semiconductor magazine Smart Techie has selected me as one of the 10-woman achievers in the field for the year 2008.

Academic Positions and other Responsibilities (Institute Level):

1. **PG Coordinator** for VLSI Design and Embedded System, Dept of ECE, BNMIT (2011-2013).
2. **Chief Coordinator** for International Conference of VLSI, Communication, Advanced Devices, Signals & Systems and Networking **(VCASAN-2013)** conducted by ECE & TCE in the year 2013.
3. **Editor** for the proceeding of International conference on VLSI Communication, Advanced Devices, Signal & Systems and Networking **(VCASAN-2013)** held at BNMIT during July 17-18, 2013.

Professional Memberships:

- **Senior Member** Institute of Electrical and Electronics Engineers (IEEE).
- **Member,** International association of computer science and information technologies (IACSIT).
- **Technical Committee Member** – IC-News, BMSCE, 2019.
- **Special invitee,** Karnataka vision group for Mysore electronics cluster for skill gap identification and development, 2019
- **Member,** BOE, VTU for ECE-TE composite board, 2012-2013.
- **Member BOS, VTU for ECE- TE composite board** 2018-2019.
- **Member BOS, NIE for ECE Mysore 2018-2019**
- **Special invitee, BOS, PES University 2018-2019**

Books:

1. Authored **"A Practical Approach to VLSI System on Chip (SoC) Design"** published by Springer Nature (In production to be released in June 2019)

2. Editor, "**Proceedings of International conference of VLSI, communication, advanced devices and Networking- VCASAN 2013"**, Published by Springer

Research Publications:

I. International Journal:

1. Shubha Rao K, Veena S Chakravarthi, **"Analysis of power conversion Efficiency of buck converter operating in continuous current mode",** Journal of Emerging Technologies and Innovative Research (ISSN: 2349-5162, UGC Approved & 5.87 Impact Factor), Volume 6, Issue 2, pp.588-593*, Feb 2019.*

2. Shubha Rao K, Mamatha S, Veena S Chakravarthi, **"FPGA Based Digital controller for DC-DC buck converter"**, *IJIRCCE*, Volume 3, ISSUE 5, pp. 4616-4623, May 2015.

3. Shubha Rao K, Veena S Chakravarthi, Soumya P Maharajanvar, **" Design of Digitally controlled switched mode power supply for low power high-frequency applications,"** *IJISET*, Volume 1, Issue 4, pp.529-532, June 2014

4. *Yasha Jyothi M Shirur,* Veena S Chakarvarthi, Kavana Hegde ***"Applying Shannon expansion concept for power optimization of digital design"***. This paper got published in International Journal of Current Engineering and Technology (IJCET)-2013.

5. Yasha Jyothi M Shirur,Veena S Chakarvarthi, ***"Design and Implementation of Power efficient Micor Pipelined GALS based 2D FFT Processor Core"*** presented in International Conference of Communication and Signal Processing, and published in International Journal of Signal Processing Systems Vol. 3, No. 2, p-p. 166-171, December 2015. DOI: 10.12720/ijsps.3.2.166-171 (IJSPS, ISSN:2315-4535; DOI: 10.12720/ijsps)

II. National/International Conference Proceedings:

1. *Vrunda Kusanur, Veena S Chakravarthi, Siddalingaiah, Founder & CEO, Precision Farming,* ***Smart Urban Rooftop Greenhouse with WSN based precision technology,*** *ICAFB-Jan 2019*

2. Shubha Rao K, Veena S chakravarthi, **"High-resolution DPWM for DC-DC buck converter using sigma-delta modulation techniques",** 7th International Conference on Applied Science, Engineering and Technology at Sri Sairam Engineering College, Anekal, Banglore, May 2nd -3rd, 2019.
3. Shubha Rao K, Veena S chakravarthi, **"Design and Performance analysis of digital control laws for low power high frequency switching power supply,***" IEEE 2nd International Conference on Power and Energy Applications (ICPEA 2019)*, Singapore, April 27-30,2019**.**

4. Shubha Rao K, Abhinav Prabhu, Veena S Chakravarthi, **"Design of FPGA-Based Sliding mode controller for Low-voltage High-frequency Buck converter",** *IEEE-International conference on Power and Advanced Control Engineering (ICPACE)*, Bangalore, India, pp 147-151, 12-14 August 2015.

5. Shubha Rao K, Veena S chakravarthi, **"FPGA implementation of voltage regulator module for System On Chip,"** *IEEE sponsored 2nd International Conference on Electronics and Communication Systems*, Coimbatore, pp.297-302, 26 & 27 February 2015.

6. Shubha Rao K, Veena S Chakravarthi, **"Digital Modeling of Switching Mode Power Supply for SOCs,"** *International Conference on Electrical Computer and Communication Engineering (ICECCE)*, pp 929-934, Paris, 14-16 Nov 2011.
7. *Yasha Jyothi M Shirur, Chetana Bilure, Veena S Chakravarthi* ***"Performance analysis of low power microcode based asynchronous P-MBIST"*** Presented in 4th International conference on Advances in computing, communications & Informatics. (ICACC-2015) conducted during 10-

13th August in Aluva Kochi, India and got published in IEEE Xplore Digital Library. P-P 555-560 DOI: 10.1109/ICACCI.2015.7275667, ISBN: 978-1-4799-8792-4/15 with impact factor 5.629.

8. Yasha Jyothi M Shirur, Veena S Chakarvarthi, Lakshmi H R ***"Implementation of Area Efficient Hybrid MBIST for Memory clusters in Asynchronous SoC"*** Presented in Fifth International Symposium on Electronic System Design(ISED- 2014) conducted during 15-17 December 2014 in Surathkal, Mangalore, India and got published in IEEE Computer Society. P-P 226 - 227 DOI:10.1109/ISED.2014.57.
9. Vanishree P, Veena S Chakravarthi, ***"A Design and Implementation of Voice Morphing on FPGA"***, International Conference on Electronics and Communication 2013, IRD Bangalore,24th April'2013.
10. Gourav Thakur, Veena S. Chakravarthi, ***"Design and Performance Analysis of 8-bit Asynchronous Pipelined Processor"***, Students Proceedings of International Conference on VLSI, Communication, Advanced Devices, Signals & Systems and Networking (VCASAN-2013), BNMIT, Bangalore 17-19, July2013.
11. Veena S Chakravarthi, Mr. Kiran K N, Nikitha S, Pavan N Bharadwaj, Ridhimaa M, Srinidhi S, ***"Design and Implementation of Audio Processor Core",*** Students Proceedings of International Conference on VLSI, Communication, Advanced Devices, Signals & Systems and Networking (VCASAN-2013), BNMIT, Bangalore 17-19, July2013.
12. Veena S Chakravarthi, ***"Platform SOC for SMART Home"*** Proceedings of International Conference on VLSI, communication, Advanced Devices, Signals & Systems and Networking (VCASAN-2013), SPRINGER, BNMIT, Bangalore 17-19,July2013,pp.31-33.
13. Yasha Jyothi M Shirur, Veena S Chakarvarthi, Varchaswini R ***"Adder based Address generator for Embedded Memories"*** presented in International Conference of VLSI, Communication, Advanced Devices, Signals & Systems and Networking (VCASAN-2013). This paper got published in lecture Notes in Electrical Engineering 258 Springer Proceedings.
14. D.N. Krishna Kumar, R.S. Rajan, Veena S Chakravarthi, ***"Determining Standard Cell Drive Strength Based on On-Chip Load Assessment"*** Proceedings of International Conference on VLSI, Communication, Advanced Devices, Signals & Systems and Networking (VCASAN-2013), SPRINGER, BNMIT, Bangalore 17- 19, July2013, pp.117-123.
15. V.S. Chakravarthi, BNMIT and S. Ghosh, University of South Florida, ***"Circuit Design Methodologies for Test Power Reduction in Nano-Scaled Technologies",*** Proceedings of International Conference on VLSI, Communication, Advanced Devices, Signals & Systems and Networking (VCASAN-2013).
16. V.S. Chakravarthi and M. Shilpa, ***"Ingress Flow Based Triple Token Bucket Traffic Control System for Distributed Networks"***, Proceedings of International Conference on VLSI, Communication, Advanced Devices, Signals & Systems and Networking (VCASAN-2013), SPRINGER, BNMIT, Bangalore 17-19, July 2013,pp.133-13
17. Yasha jyothi M Shirur, Veena S Chakravarthi,Gourav Thakur, ***"Performance Analysis of 8 bit pipelined Asynchronous Processor Core"*** presented in an IP-SoC-2013, Grenoble, France.
18. Shiva Kumar K, YashaJyothi M Shirur, Veena S Chakravarthi, ***"Reliable Boundary Scan Insertion Methodology for Multi-Chip Module Based Designs"*** presented in International Conference on VLSI and Signal published in ICVSP-2012 Proceeding, May 4-5th 2012, pp.113-118.
19. Prabhavathi P, Veena S Chakravarthi, B N M Institute of Technology, ***"At Speed scan test Challenges and Future Scope of work - A Survey"*** - INCOMM10-AtSpeedTestSoc. 9-4-2010, Indore.

20. Veena S Chakravarthi, Kumar M N, K S Gurumurthy, UVCE, ***"Auto SoC Top design integration"***, IPSoC 2008 Grenoble, France.
21. Veena S Chakravarthi, ***"SoC Design – A Walk Through"*** –NOVAS USER Conference, Bangalore 2007.
22. Veena S Chakravarthi, Kumar MN, Dinesh A, Centillium India Pvt. Ltd., K S Gurumurthy, UVCE, ***"Timing closure with low power advantage for ASSP designs"*** IPSoC- 2007 Grenoble, France
23. Veena S Chakravarthi, Kumar M N, ***"SOC debug using Novas Verdi – An Experience";*** NOVAS USER Conference 2006.
24. Veena S Chakravarthi, Dinesh A, Centillium India Pvt. Ltd***.,"GUI based Complex SoC Verification environment using TCP/IP based socket"***, SNUG2005.
25. Veena S Chakravarthi, Centillium India Pvt. Ltd., K S Gurumurthy, UVCE, ***"Power Optimization techniques for Core based SoC designs"*** IPSoC- Dec 2005, Grenoble, France.
26. Veena S Chakravarthi, Vilas Bhade, Mindtree Consulting Pvt. Ltd., KS Gurumurthy, Professor, UVCE, ***"SoC Design strategies"*** –VDAT Bangalore2001.

Professional associations and invited talks

- Vice Chair, IEEE Nano Technology council, Bangalore section for 2018-2020.
- Successfully closed the collaboration as academic research partner between BNM Institution and Sensesemi Technologies Pvt. Ltd.
- Invited talks on **"Healthcare trends and challenges"** at Cadence design systems
- Invited talk on **"Medtech devices -Challenges of Making in India"** Product design and innovation workshop, UVCE, Feb'2019
- Invited talk on **"Communication at the speed of light",** NIE Mysore 2018
- Invited Talk on "***Diabetes monitoring using Sensesmart health eco system"***, Diabetes congress Dubai, Dec5,2018

Visits Abroad:

1. **Grenoble, France: Chaired session on VLSI; IPSOC 2013**
2. **Grenoble, France:** To present research paper on ***"Performance Analysis of 8-bit pipelined Asynchronous Processor Core"*** in IPSoC-2013 from 1st to 11th November 2013.
3. **Bangkok, Thailand:** To present research paper on ***"Design and Implementation of Power efficient Micro Pipelined GALS based 2D FFT Processor Core*** in ICCSP-2014.
4. **Dubai:** Moderator, Diabetes Congress Dec 4-5, 2018

Personal Details:

- **Date of Birth:** 20-07-1964
- **Gender**: Female.
- **Family Details:** Married and have two sons

15th May 2019 **DR. VEENA S CHAKRAVARTHI**