Faculty Profile

Name of Faculty	Dr. Yasha Jyothi M Shirur
Department	Electronics and Communication Engineering
Qualification	BE, M.Tech, Ph.D
Designation	Professor
Area of specialization	VLSI, Design for Testability
Date of Joining BNMIT	17/01/2004
Nature of Association	Regular
e-mail	yashamallik@gmail.com yashajyothimshirur@bnmit.in
No. of years of Experience	18 years

Academic Qualifications:

- **Ph.D.** (2017), Department of Electronics and Communication Engineering, Visvesvaraya Technological University, India.
- **M.Tech.** (2004), Electronics, B M S College Of Engineering, Visvesvaraya Technological University, India.
- **B.E.** (1997), Bapuji Institute of Technology, Davangere, Kuvempu University, Karnataka, India.

Working Experience Details:

- **Professor,** Dept. of Electronics and Communication Engineering, BNMIT, Bangalore, India, (2017 -Till date).
- **Associate Professor**, Dept. of Electronics and Communication Engineering, BNMIT, Bangalore, India, (2012-2017).
- **Assistant Professor**, Dept. of Electronics and Communication Engineering, BNMIT, Bangalore, India, (2008-2012).
- **Lecturer,** Dept. of Electronics and Communication Engineering, BNMIT, Bangalore, India, (2003-2008).
- **Teaching Assistant**, Dept. of Telecommunication Engineering, DSCE, Bangalore, India, and (2001-2002).
- **Faculty**, CMS Computer Institute, Davangere, Karnataka, India (1997-1999).

Research Experience Details:

Ph.D:

Designed of A-SoC(Zeus A-SoC) consisting of A-RISC Processor Core, A-DSP Processor Core, 2-D FFT Engine, defined test techniques for A-SoC, filed patent on Asynchronous System on Chip Test through JTAG: Testing of asynchronous blocks with handshake pipelines (protocol) in A-SoC, through JTAG is proposed and implemented. Inserting asynchronous JTAG test logic speeds up the test process is functionally verified.

Patent Filed:

- Patent Pending with patent no: 201641022110.
- **Title:** "Method, System and Apparatus for Asynchronous SoC Testing and Validation"
- **Inventors:** Yasha Jyothi M Shirur, Dr. M. S. Suresh, Dr. Veena S Chakaravarthi**.**

Subjects taught:

- CMOS VLSI Design, ASIC Design, Digital VLSI Design, Design of VLSI System, Analog mixed mode VLSI Design SoC Design, VLSI Testing and Verification, VLSI Testing, Advances in VLSI Design, Basic Electronics, Analog Electronics Circuits, Network Analysis, Linear Integrated circuits and applications, Principles of Communication System, Transmission Lines and Waveguides, Information Theory and Coding, Digital Communication, Digital design using Verilog, Programming with C++, Cryptography and network security.

Academic Positions and other Responsibilities (University Level):

1. **Deputy Chief Superintendent** (External) at BMSCE, Bangalore for the conduction of January 2012 B.E. examinations of VTU, Belgaum.
2. **Deputy Chief Superintendent** (External) at DSCE, Bangalore from 17-07-2017 to 2-08-2017 for the conduction of June 2017 B.E. examinations of VTU, Belgaum.

Academic Positions and other Responsibilities (Institute Level):

1. **Faculty Development Program Convener** for "IoT based Project Design and development" held during 24th to 29th June, 2019.
2. **Chief Test Coordinator**, BNMIT (2017-2018).
3. **Member,** Anti ragging Squad, BNMIT (2017-18).
4. **Coordinator**, TATVA, BNMIT (2016-2017).
5. **PG Coordinator** for VLSI Design and Embedded System, Dept of ECE, BNMIT (2016-till date).
6. **Technical session coordinator** for International Conference on Fluid Dynamic and its Applications **(ICFD-2017)** conducted by mathematics department from July 12-14 2017.
7. **Pre-Conference Tutorial Coordinator** for International Conference on Power and Advanced Control Engineering **ICPACE-2015.**
8. **Coordinator** for International Conference of VLSI, Communication, Advanced Devices, Signals & Systems and Networking **(VCASAN-2013)** conducted by ECE & TCE in the year 2013.
9. **Editor** for the proceeding of International conference on VLSI Communication, Advanced Devices, Signal & Systems and Networking **(VCASAN-2013)** held at BNMIT during July 17-18, 2013.

Awards/ Achievements/Memberships:

- **Merit Award** received while pursuing M.Tech in 2003 at BMSCE, Bangalore.
- **Best Oral Presenter Award** for Best Presentation in International Conference of Communication and Signal Processing (ICCSP-2014), Bangkok, Thailand.

Professional Memberships:

- **Secretary**, IEEE Nano Tech Council, Bengaluru Section, Bengaluru, Karnataka, India.
- **Life Member**, Indian Society for Technical Education (ISTE) with Membership No. - LM50243.
- **Member,** Institute of Electrical and Electronics Engineering (IEEE) with Membership No. 92819949.

Research Publications: 34

I. International Journal: 16

1. Yasha Jyothi M Shirur ***"Efficient Method to Measure Dynamic Temperature Variations in an Non Uniform Heat Dissipated Integrated Chip"*** got published in International Journal of Computer Sciences and Engineering. (IJCSE) Vol.-7, Issue-6, Jun 2019.
2. Yasha Jyothi M Shirur, Harshitha A "**An Efficient Radix-3 Multiplierless 2D Convolution Filter for Visual Search Applications"** got published in International Journal of Scientific Research and Review (IJSR) ISSN NO: 2279-543X, Volume 8, Issue 5, May 2019, pp-650-654.
3. Sujaya H S, Suchit Shavi, Rohith J Bharadwaj, Yasha Jyothi M Shirur "***Anger Detection Module for Assisting Dementia Patients"*** got published in International Journal of Innovative Research in Science, Engineering and Technology. (IJIRSET) Vol. 7 Issue: 6 July 2018 with ISSN (Online): 2319-8753 and Cross ref - DOI:10.15680/IJIRSET.2018.0706091 & impact Factor 7.089.
4. Yasha Jyothi M shirur ***"Wireless Local Area Network Frame Classification to Access Categories based on User Priority"*** got published in International Journal of Innovative Research in Science, Engineering and Technology. (IJIRSET) Vol. 7 Issue: 6 June 2018 with ISSN (Online): 2319-8753 and Cross ref - DOI:10.15680/IJIRSET.2018.0706091 & impact Factor 7.089.
5. Anu K L, Yasha Jyothi M Shirur, and Mr. Prasannakumar Y ***"Design and Implementation of Driver Assistance System (Das) Using Raspberry Pi to Enhance Driver Safety"*** in International Journal of Engineering Research & Technology (IJERT) Vol. 5 Issue: 04 April 2018 with ISSN: 2395-0056.
6. Amshu Vinayak. T, Yasha Jyothi M Shirur "***Automatic Control for Greenhouse Farming"*** got published in International Journal of Engineering Research & Technology (IJERT) Vol. 6 Issue: 09 September 2017 with ISSN: 2278-0181 and Cross ref - DOI Prefix: 10.17577.
7. Kritika M Sharma Aishwarya A, Yasha Jyothi M Shirur ***"Power Efficient Destination Address Generator of Direct Memory Access Controller in Multiprocessor SoC"*** got published in International Journal of Innovative Research in Computer and Communication Engineering (IJIRCCE) Vol. 5, Issue: 7 July 2017 with ISSN:2320-9801 and impact factor 6.577.
8. Akhila K Karuna N Kavya C, Yasha Jyothi M Shirur ***"Design and implementation of Power Efficient Linear Feedback Shift Register for BIST using Verilog"*** got published in International Journal of Innovative Research in Computer and Communication Engineering (IJIRCCE) Vol. 5, Issue: 7 July 2017 with ISSN:2320-9801 and impact factor 6.577.
9. Sagar R, Yasha Jyothi M Shirur ***"Efficient Trash Management System Using Smart Bin"*** got published in International Research Journal of Engineering and Technology (IRJET) Vol. 4, Issue: 5 May 2017 with ISSN: 2395-0056 and impact factor 5.181.
10. K Shreshta Subodh Shetty, Yasha Jyothi M Shirur ***"Video Oculographic System enabling Communication for Patients suffering from Motor Neuron Disease"*** got published in Perspective in Communication, Embedded-Systems and Signal-Processing Vol. 1, Issue 2 May 2017 p-p 19-21.
11. *Nikitha Teggi, Yasha Jyothi M Shirur, Vishweshwar Mundkur* ***"Modeling of LORA Transceiver in MATLAB using SIMULINK"*** IJMER Vol. 3, No. 6, 166-171, 159-162 with impact factor 3.518.

12. Yasha Jyothi M Shirur,Veena S Chakarvarthi, ***"Design and Implementation of Power efficient Micor Pipelined GALS based 2D FFT Processor Core"*** got published in International Journal of Signal Processing Systems Vol. 3, No. 2, p-p. 166-171, December 2015. DOI: 10.12720/ijsps.3.2.166-171 (IJSPS, ISSN:2315-4535;DOI: 10.12720/ijsps.
13. Ranjith Kumar M, Yasha Jyothi M Shirur, Ramudu B "***Development of Verification Environment to Verify CSR Registers for DDR4 Memory Controller through APB Interface Using UVM Methodology"***, ISSN 2394-3785 Available online at www.ijartet.com International Journal of Advanced Research Trends in Engineering and Technology (IJARTET) Vol. II, Special Issue XXVII, June 2015 in association with Dayananda Sagar College Of Engineering, National Conference On "Emerging Trends In VLSI, Embedded System, Nano Electronics And Telecommunication System" DSCE NCEVENT'15 JUNE 16 & 17,2015 58_62 All Rights Reserved © 2015 IJARTET.
14. Yasha Jyothi M Shirur, Lakshmi H R, Varchaswini R ***"Implementation of FSM-MBIST and Design of Hybrid MBIST for memory cluster in Asynchronous SoC***". This paper got published in International Journal of Computer Applications Technology and Research IJCAT- Volume 3– Issue 4, 216 - 220, 2014.
15. Nishanti G, Yasha Jyothi M Shirur, Ramudu B ***"Functional coverage for low power DDR2 Memory Controller in UVM".*** This paper got published in International Journal of Computer Applications Technology and Research IJCAT- Volume 3– Issue 5, 292 - 295, 2014.
16. Yasha Jyothi M Shirur, Veena S Chakarvarthi, Kavana Hegde ***"Applying Shannon expansion concept for power optimization of digital design"***. This paper got published in International Journal of Current Engineering and Technology (IJCET)-2013.

II. National Journals: 4

1. Nishanti G, Yasha Jyothi M Shirur, Ramudu B "***Coverage driven verification environment development of low power ddr2 memory controller***" Published in National Conference proceedings on VLSI, Image processing and Networking, Indira Institute of Technology, Chennai. 22-27 held on 28th of April 2014.
2. Kumarswamy, Yasha Jyothi M Shirur, Veena S Chakarvarthi***" Implementation of Logic BIST for any Digital Core***" presented in National Conference on Recent Advances in Electronics and Communication Engineering conducted during May 2013.
3. Sindhu, Yasha Jyothi M Shirur "***Implementation of all digital phase locked loop with input fault detection"*** presented in National Conference on Recent Advances in Electronics and Communication Engineering conducted during May 2013.
4. Dharmendra N Kerur, Yasha Jyothi M Shirur, S.B. BhanuPrashanth ***"Design of mixed signal cmos-pll with improved acquisition and its application as frequency synthesizer" p***resented in National Conference on Recent Trends in Industrial Electronics and Instrumentation CRTIEAI-2013 conducted during 7th June 2013.

III. National/International Conference Proceedings: 14

1. Yasha Jyothi M Shirur, Kritika M Sharma, Aishwarya A "***Design and implementation of Efficient Direct Memory Access (DMA) Controller in Multiprocessor SoC"*** presented in International Conference on Networking Embedded and Wireless System (ICNEWS-2018) held on 27th and 28th of December 2018 and got published in IEEE Xplore Digital Library. 978-1-5386-7949-4/18/2018.

2. Akhila K, Karuna N and Yasha Jyothi M Shirur "***Design and Implementation of Power Efficient Logic BIST With High Fault Coverage Using Verilog"*** presented in International Conference on Networking Embedded and Wireless System (ICNEWS-2018) held on 27th and 28th of December 2018 and got published in IEEE Xplore Digital Library. 978-1-5386-7949-4/18/2018.
3. Yasha Jyothi M Shirur Ujwal S S, Sana Anaum, Suhas N Bhargav Zeeshan Saquib ***"Blinkom: A Smart Solution for the MND Patients"*** in 3rd IEEE International Conference on Recent Trends in Electronics, Information & Communication Technology (RTEICT-2018), MAY 2018.
4. *Chaitrashree K*, Yasha Jyothi M Shirur, Vishweshwar Mundkur ***"SIMULINK Modeling of blood pressure system"*** *got* published in Proceedings of 26th IRF International Conference PP-9-12 ISBN: 978-93-86083-38-8. International Conference on Engineering and Technology held on 12th June 2016.
5. Swathi S, Ramya Jagadish, Pankaja K, Yasha Jyothi M Shirur ***"Fault Tolerant carry select Adder and Dadda Multiplier using Reversible Logic Technique"*** got published Conference Proceedings with ISBN: 978-81-92958-06-1. International Conference on Emerging Trends in Engineering and Technology [IFERP] held on 22nd May 2016.
6. Yasha Jyothi M Shirur, Shurthi S "***Implementation of IEEE 1687 standard for Access Instrumentation using Verilog"*** presented in International Conference on Signal Processing, Communication and Computational Research got published in Institute of Engineering Research & Publication IFERP Proceedings, May 18th and 19th 2016.
7. *Yasha Jyothi M Shirur, Chetana Bilure, Veena S Chakravarthi* ***"Performance analysis of low power microcode based asynchronous P-MBIST"*** Presented in 4th International conference on Advances in computing, communications & Informatics. (ICACC-2015) conducted during 10-13th August in Aluva Kochi, India and got published in IEEE Xplore Digital Library. P-P 555-560 DOI: 10.1109/ICACCI.2015.7275667, ISBN: 978-1-4799-8792-4/15 with impact factor 5.629.
8. YashaJyothi M Shirur, Suhasin Hegde, Vindhya Adiga, Rakshith G R and Priyanka S Bhat **"*IEEE Standard 1149.1 Boundary Scan Insertion Methodology for Power Efficient Asynchronous 8 bit Processor Core"*** presented in International Conference on VLSI and Signal Processing and got published in ICVSP-2014 Proceedings , August 13th and 14th 2014.
9. Yasha Jyothi M Shirur, Veena S Chakarvarthi, Lakshmi H R ***"Implementation of Area Efficient Hybrid MBIST for Memory clusters in Asynchronous SoC"*** Presented in Fifth International Symposium on Electronic System Design (ISED- 2014) conducted during 15-17 December 2014 in Surathkal, Mangalore, India and got published in IEEE Computer Society. P-P 226 - 227 DOI:10.1109/ISED.2014.57.
10. Yasha Jyothi M Shirur Mrs. Rekha P "***Towards A Hybrid Pan sharpening Algorithm For High Resolution Satellite Imagery***" Presented in Fourth International Conference of Communication and Signal Processing (ICCSP-2015) conducted during 2-4th April 2015 in Melmaruvathur, Tamilnadu, India and got published in IEEE Xplore Digital Library P-P 1252 - 1256 DOI:10.1109/ICCSP.2015.7322708.
11. Yasha Jyothi M Shirur, Veena S Chakarvarthi, Varchaswini R ***"Adder based Address generator for Embedded Memories"*** presented in International Conference of VLSI, Communication, Advanced Devices, Signals & Systems and Networking (VCASAN-2013). This paper got published in lecture Notes in Electrical Engineering 258 Springer Proceedings.

12. Dharmendra N Kerur, Yasha Jyothi M Shirur, S.B BhanuPrashanth ***"Design of 1GHz Mixed Signal CMOS-PLL with Fast Phase and Frequency Acquisition" p***resented in International Conference on VLSI, Communication, Advanced Devices, Signals & Systems and Networking (VCASAN-2013) conducted during 17-19 July 2013. This paper got published in VCASAN-2013 Proceedings.
13. Yasha Jyothi M Shirur, Veena S Chakravarthi, Gourav Thakur, ***"Performance Analysis of 8 bit pipelined Asynchronous Processor Core"*** presented in an IP-SoC-2013, Grenoble, France.
14. Shiva Kumar K, Yasha Jyothi M Shirur, Veena S Chakravarthi, "***Reliable Boundary Scan Insertion Methodology for Multi-Chip Module Based Designs"*** presented in International Conference on VLSI and Signal published in ICVSP-2012 Proceeding, May 4-5th 2012, pp.113-118.

Participation in Training courses/Seminars/Workshops

1. ***"MSP430 and its applications"*** FDP conducted by BNMIT, Bangalore in association with ALS, Bengaluru from 31st July to 5th August 2017.
2. ***"Physical Design Challenges in DSM Node VLSI Systems"*** FDP conducted by BNMIT, Bangalore in association with Cadence Bengaluru on 16th - 21st January 2017**.**
3. ***"Computer and Wireless Networks"*** FDP conducted by BNMIT, Bangalore in association with IEEE Communication Society Bangalore Chapter on 11th-16th July 2017**.**
4. ***"ARM Cortex M3"***FDP conducted by BNMIT, Bangalore in association with TRONIKBIT TECH LLP Bengaluru 8th to 14thJanuary 2016**.**
5. ***"Innovative Teaching Methods"*** Organized by BNMIT in association with National Institute of Technical Teachers Training & Research Chennai, Government of India, Ministry of Human Resource Development, 18th to 23rd July 2016.
6. ***"DFT Methodology"*** training in Asarva Chips and Technology Pvt. Ltd., Bangalore from 16th to 25th June 2016.
7. ***"Tech Treat on Emerging Technologies"*** Symposium conducted by IEEE Student chapter in association with IEEE Nano Tech Council on 4th and 5th of August 2016 at BNMIT.
8. ***"IoT Hands on Workshop for Beginners "***conducted by IED Forum on 13th and 14th June 201.5
9. ***"Innovus Implementation System"*** conducted by Cadence on 6th May 2015.
10. *"**IpSoc-2015"*** conducted by Design & Reuse on 25th March 2015.
11. ***"Hands on Training"*** workshop conducted by IISc, Bangalore under INUP Program from 3rd-12th February 2015.
12. ***"Digital Font End Design and Implementation using Synopsys Tools"*** Organized by BMSCE in association with Chip Edge Technologies Pvt. Ltd. Bangalore held during 13th-25th January 2014.
13. *"**Protium Rapid Prototyping Platform FPGA-based prototyping Solution"*** Conducted by Cadence during 4th September 2014.
14. ***"Internalize Intellectual Property & Strategic management of Intellectual property Rights"*** Organized by Entrepreneurship Development Cell VTU, Belgaum, during 2nd March 2012.
15. ***"Innovative Teaching & Effective Communication"*** organized by BNMIT held during 18th-20th of July, 2012.
16. ***"Digital Design using Verilog"*** Tutorial organized by BNMIT, Bangalore during 19th-21st of Oct 2012.
17. **"SoC Design – a walk through"** conducted by BNMIT during 17th-19th January 2011.

18. **"*High Impact on Teaching Skills – MISSION10X"*** conducted by WIPRO in association with ISTE during 19th-23rd July 2010.
19. ***"MEMS Software Training Program"*** conducted by IISc during 24th-28th of May 2010.
20. ***"Analog & Mixed mode IC design A Practical Approach"*** conducted by M S Ramaiah School of Advanced Studies during 12th-14th of March 2009.
21. ***"Faculty development program on MEMS"*** conducted by MSRIT during 21st-26th of December 2009.
22. ***"Analog and Mixed Mode Design Using Cadence Tool"*** conducted by BNMIT during 2nd - 4th of Feb 2009.
23. ***"Technical Education Quality Improvement Programme - on Wireless Communication Technology and Trends"*** conducted by BMSCE during 23rd and 24th March 2007.
24. ***"Quality Improvement Programme- Instructional Design and Delivery"*** conducted by National Institute of Technical Teachers Training & Research during 9th–14th August 2004.
25. ***"Faculty Training Programme on Advanced Electronic Laboratories"*** conducted by RNSIT during 10th -15th February 2004.
26. ***"Research Workshop on Signal and Image Processing"*** conducted by BNMIT during 28th and 29th of January 2010.
27. ***"Research Methodologies and Report Writing"*** conducted by e-learning centre, Mysore during May 28th and 29th of 2009 at MSRIT.

Visits Abroad:

1. **Grenoble, France:** To present research paper on ***"Performance Analysis of 8 bit pipelined Asynchronous Processor Core"*** in IPSoC-2013 from 1st to 11th November 2013.
2. **Bangkok, Thailand:** To present research paper on ***"Design and Implementation of power efficient Micor Pipelined GALS based 2D FFT Processor Core*** in ICCSP-2014.

Personal Details:

- **Date of Birth:** 19 -06 –1974
- **Gender**: Female.
- **Marital Status:** Married and have two children.

23rd July 2018 **DR.YASHA JYOTHI M SHIRUR**