B N M Institute of Technology

An Autonomous Institution under VTU. Approved by AICTE

Department: Electronics and Communication Engineering

Scheme of Teaching and Examination - Autonomous Effective from Academic year 2023-24

III Semester M. Tech (VLSI Design and Embedded Systems)

Sl. No	Course Type	Course Code	Course Title		Teaching Department	Teaching Hours /Week					Examination			
						L	T	P	J	Hours /Week	Credits	CIA Marks	SEA Marks	Total Marks
1	PCC	23VDE231	CMOS RF Circuits Design		ECE	3	-	-	-	3	3	50	50	100
2	PCC	23VDE232	CAD for Digital Systems		ECE	3	-	-	-	3	3	50	50	100
3	PEC	23VDEP233X	23VDEP2331	VLSI Design for Signal Processing	ECE	3	-	-	-	3	3	50	50	100
	PEC		23VDPE2332	Machine Learning using Python			-	-	-					
	PEC		23VDEP2333	Synthesis and Optimisation of Digital Circuits			-	-	-					
4	PEC	23VDEP234X	23VDEP234X	MOOC/NPTEL (Subjected to offering by NPTEL)	ECE	3	-	-	-	3	3	50	50	100
5	INT	23VDEI235	Internship			-	-	6	-	6	3	50	50	100
6	PRJ	23VDEJ236	Project Work Phase-1			-	-	-	10	10	5	100	0	100
TOTAL						12	-	6	10	28	20	250	350	600

Summer Internship to be carried out during the vacation between II & III Semester

Summer Internship - I (23VDEI235): All the students registered to II year of M.Tech shall have to undergo mandatory internship of 6 weeks between II semester or III semester vacation. Semester End Assessment will be conducted in III semester and the prescribed credit will be included. Internship shall be considered as a head of passing and shall be considered for the award of degree. Those, who do not take up / complete the internship shall be declared fail and shall have to complete during subsequent examination after satisfying the internship requirements. (The faculty coordinator or mentor has to monitor the students' internship progress and interact to guide them for the successful completion of the internship.)

Project work: Phase-1 (23VDEJ236): Based on the abilities of the students and recommendations of the mentor, a single discipline or a multidisciplinary project can be assigned to an individual student. The progress of the project work will be evaluated continuously. There will be 2 seminars in 2 phases, evaluated by a panel of faculty members with HOD as the Chairperson.

M. Tech. (VLSI Design & Embedded System) Choice Based Credit System (CBCS and Outcome Based Education (OBE)		
Semester: 3		
Course Name: CMOS RF Circuits Design		**Course Code: 23VDE231**
L: T: P: J	**3:0:0:0**	**CIA Marks: 50**
Credits:	**3**	**SEA Marks: 50**
Hours/Week (Total)	**3**	**SEA Duration:** 03 Hours

Course Learning Objectives: The students will be able to

1	Learn basic concepts in RF and microwave design emphasizing the effects of nonlinearity and noise.
2	Appreciate communication system, multiple access techniques and wireless standards necessary for RF circuit design.
3	Deal with transceiver architecture, various receiver and transmitter designs, their merits and demerits.
4	Understand the design of RF building blocks such as Low Noise Amplifiers, Mixers.
5	Understand the working principal of Oscillators, VCOs, Frequency Synthesizers and PLLs

Module 1: Introduction to RF Design, Wireless Technology and Basic Concepts	**No. of Hours**	**Blooms cognitive Levels**
A wireless world, RF design is challenging, The big picture. General considerations, Units in RF Design, Time Variance, Nonlinearity, Effects of Nonlinearity, Harmonic Distortion, Gain Compression, Cross Modulation, Intermodulation, Cascaded Nonlinear Stages, AM/PM Conversion, Noise, Noise as a Random Process, Noise Spectrum, Effect of Transfer Function on Noise, Device Noise, Representation of Noise in Circuits.	**8**	**Apply CO1**
Module-2 Passive Impedance Transformation and Communication Concepts		
Passive Impedance Transformation: Quality Factor, Series-to-Parallel Conversion, Basic Matching Networks, Loss in Matching Networks. **Communication Concepts:** General concepts, analog modulation, digital modulation, spectral re-growth. Mobile RF communications, Multiple access techniques, Wireless standards Specifications only.	**8**	**Apply CO2**
Module-3 Transceiver Architecture		
Receivers: General Considerations, Receiver Architectures, Basic Heterodyne Receivers, Modern Heterodyne Receivers, Direct-Conversion Receivers, Image-Reject Receivers. **Transmitters**: Transmitter Architectures, General Considerations, Direct-Conversion, Transmitters, Modern Direct-Conversion Transmitters, Heterodyne Transmitters.	**8**	**Apply CO3**
Module-4 Low Noise Amplifiers and Mixers		
Low Noise Amplifiers: General considerations, Problem of input matching, LNA topologies: common-source stage with inductive load, common-source stage with resistive feedback, Common Gate stage (only upto Input impedance). **Mixers:** General considerations, Performance parameters, Mixer Noise Figures, Single balanced and Double balanced mixers, Passive download Mixers, Gain, LO self-mixing, Noise, Input Impedance, Current driven passive mixers.	**8**	**Apply CO4**
Module-5 VCO, PLLs and Power Amplifiers		
VCOs: Voltage-Controlled Oscillators (VCOs), Tuning Range Limitations, Effect of Varactor Q, Phase Noise, Basic Concepts, Effect of Phase Noise, Design Procedure, Low-Noise VCOs, LO Interface, Quadrature Oscillators, Basic Concepts **Phase-Locked Loops (PLLs):** Basic Concepts, Phase Detector, TYPE-I PLLS, Alignment of a VCO's Phase, Simple PLL, Analysis of Simple PLL, Loop Dynamics, Frequency Multiplication, Integer-N Frequency	**8**	**Apply CO5**

Synthesizers, General Considerations, Basic Integer-*N* Synthesizer **Power Amplifiers:** General Considerations, Classification of Power Amplifiers, Class A Power Amplifiers, Class B Power Amplifiers, Class AB Power Amplifiers, Class C Power Amplifiers		

Course Outcomes: After completing the course, the students will be able to	
23VDE231.1	Analyze the effect of nonlinearity and noise in RF and microwave design.
23VDE231.2	Understand communication system, multiple access techniques and wireless standards necessary for RF circuit design.
23VDE231.3	Describe various receivers and transmitter topologies with their merits and drawbacks.
23VDE231.4	Design Mixers and Low-Noise Amplifiers with minimum number of off-chip components.
23VDE231.5	Exemplify the approaches taken in the design of VCOs, PLLs, Frequency synthesizers and Power amplifiers.
23VDE231.6	Illustrate how the system requirements define the parameters of the circuits and the impact on the performance.

Reference Books

1. RF Microelectronics, B. Razavi, PHI, second edition.
2. CMOS Circuit Design, layout and Simulation, R. Jacob Baker, H.W. Li, D.E. Boyce, PHI 1998

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<tr><td>Assignment</td><td colspan="2">15</td></tr>
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i) CIA: 50%

IA Test: 2 IA tests - Each of 50 Marks	Average of 2 tests – scaled down to 25 M
Assignment – Two assignments – one for 10 marks and another for 5 marks	15 Marks
Additional Assessment Tools (AAT) – Oral /Online Quizzes, Presentations, Group discussions, Case studies, Term Paper, Open ended experiments, Mini industrial/social/rural Projects, Two-minute video on latest topic, Short MOOC courses, Practical Orientation on Design thinking, creativity & Innovation, Participatory & Industry integrated learning, Practical activities, Problem solving exercises, Participation in seminars/academic events/symposia and any other activity	10 Marks
Total	**50 Marks**

ii) SEA: 50%

Theory Exam	5 questions to answer each of 20 Marks 2 questions from each module with internal choice Student should answer one full question from each module	20 M x 5 = **100 M reduced to 50 M**
	Total	**50 Marks**

M. Tech. (VLSI Design & Embedded System) Choice Based Credit System (CBCS and Outcome Based Education (OBE)		
Semester: III		
Course Name: CAD for Digital Systems		**Course Code: 23VDE232**
L: T: P: J	**3:0:0:0**	**CIA Marks: 50**
Credits:	**3**	**SEA Marks: 50**
Hours/Week (Total)	**3**	**SEA Duration:** 03 Hours
Pre-Requisites: Digital electronics		

Course Learning Objectives: The students will be able to

1	To use the algorithms of Graph theory for optimization and satisfiability.
2	To be able to differentiate between P, NP and NPC problems
3	To use graph theory in physical design.
4	To understand the time and space complexities.
5	To learn various optimization methods.
6	To understand different techniques for placement and routing.

Module-1: Introduction to Design Methodologies and Graph theory	**No. of Hours**	**Blooms cognitive Levels**
The VLSI Design Problem, The Design Domains, Design Actions, Design methods and Technologies. VLSI Design Automation tools: Algorithmic and System Design, Structural and Logic Design, Transistor-level Design, Layout Design, Verification Methods, Design Management Tools. Algorithmic graph theory and computational complexity: Terminology, Data Structures for the Representation of Graphs, Computational Complexity, Examples of Graph Algorithms. Tractable and intractable problems: Decision Problems, Complexity Classes, NP-completeness and NP-hardness, Consequences.	**8**	**Understand CO1**
Module-2: Combinatorial optimization and Layout compaction		
General purpose methods for combinational optimization: Backtracking and Branch-and-bound, Dynamic Programming, Integer Linear Programming, Local Search, Simulated Annealing, Tabu Search, Genetic Algorithms, A Few Final Remarks on General-purpose Methods. Layout compaction: Design Rules, Symbolic Layout, Problem Formulation, Algorithms for Constraint-graph Compaction, Other Issues.	**8**	**Apply CO2**
Module-3: Physical Design		
Placement and partitioning: Circuit Representation, Wire-length Estimation, Types of Placement Problem, Placement Algorithm, Partitioning. Floor planning: Floorplanning Concepts, Shape Functions and Floorplan Sizing. Routing: Types of Local Routing Problems, Area Routing, Channel Routing, Introduction to Global Routing, Algorithms for Global Routing. Machine Learning in Physical Verification, Mask Synthesis, and Physical Design (Reference- 1)	**8**	**Apply CO3**
Module-4: Logic Synthesis and Simulation – I		
Logic Synthesis and Verification: Introduction to Combinational Logic Synthesis, Binary-decision Diagrams, Two-level Logic Synthesis. Simulation: General Remarks on VLSI Simulation, Gate-level Modelling and Simulation	**8**	**Apply CO4**
Module-5: Logic Synthesis – II		
High level Logic synthesis: Hardware Models for High Level Synthesis, Internal Representation of the Input Algorithm, Allocation, Assignment and Scheduling, Some Scheduling Algorithm, Some Aspects of the Assignment Problem, High-level Transformations. Sequential logic Synthesis: Finite state machine modelling – State	**8**	**Understand CO5**

minimization – completely specified and incompletely specified, Compatibility classes, State encoding, Structural representation of sequential circuits, Retiming, Extension		

Course Outcomes: After completing the course, the students will be able to	
23VDE232.1	Demonstrate knowledge and understanding of fundamental concepts in VLSI design using CAD.
23VDE232.2	Solve graph theoretical problems.
23VDE232.3	Demonstrate knowledge of computational and optimization algorithms applicable to solving CAD related problems.
23VDE232.4	Establish comprehensive understanding of the various phases of CAD for digital electronic systems, from digital logic simulation to physical design
23VDE232.5	Demonstrate the relationship between optimization during synthesis and verification with satisfiability and formal verification
23VDE232.6	Demonstrate knowledge of computational and optimization tools applicable to solving CAD related problems.

Reference Books

1. **Algorithms for VLSI Design Automation** - S H Gerez, Wiley, 2nd Edition.
2. **Synthesis and Optimization of Digital circuits –**
3. **Machine Learning in VLSI Computer-Aided Design - Elfadel**, Ibrahim (Abe) M., **Boning**, Duane S., **Li**, Xin (Eds.), Springer, 2019
4. **Advanced Logic Synthesis** - **Reis**, André Inácio, **Drechsler**, Rolf (Eds.), Springer, 2018

PCC	**CIA**	**SEA**	**CIA (50)**			**SEA** **Conduction: 100 M** **Reduced to: 50 M**
				I	II	
Conduction	50	50	Written Test	50	50	Five questions with each of 20 marks (with internal choice). Student should answer one full question from each module
				Average of two tests – 25 Marks		
			Assignment	15		
			AAT	10		
			Total – 50 marks			**Total – 50 marks**

i) CIA: 50%

IA Test: 2 IA tests - Each of 50 Marks	Average of 2 tests – scaled down to 25 M
Assignment – Two assignments – one for 10 marks and another for 5 marks	15 Marks
Additional Assessment Tools (AAT) – Oral /Online Quizzes, Presentations, Group discussions, Case studies, Term Paper, Open ended experiments, Mini industrial/social/rural Projects, Two-minute video on latest topic, Short MOOC courses, Practical Orientation on Design thinking, creativity & Innovation, Participatory & Industry integrated learning, Practical activities, Problem solving exercises, Participation in seminars/academic events/symposia and any other activity	10 Marks
Total	**50 Marks**

ii) SEA: 50%

Theory Exam	5 questions to answer each of 20 Marks 2 questions from each module with internal choice Student should answer one full question from each module	20 M x 5 = **100 M reduced to 50 M**
	Total	**50 Marks**

M. Tech. (VLSI Design & Embedded System)
Choice Based Credit System (CBCS and Outcome Based Education (OBE)

Semester: 3

Course Name: VLSI Design Signal Processing **Course Code: 23VDEP2331**

L: T: P: J	**3:0:0:0**	**CIA Marks: 50**
Credits:	**3**	**SEA Marks: 50**
Hours/Week (Total)	**3**	**SEA Duration:** 03 Hours

Course Learning Objectives: The students will be able to

1	Learn several high-level architectural transformations that can be used to design families of architectures for a given algorithm.
2	Deal with high-level algorithm transformations such as strength reduction, look-ahead and relaxed look-ahead

Module 1	**No. of Hours**	**Blooms cognitive Levels**
Introduction to DSP Systems: Typical DSP Algorithms, DSP Application Demands and Scaled CMOS Technologies, Representations of DSP Algorithms. **Iteration Bounds:** Data flow graph Representations, loop bound and Iteration bound. Algorithms for Computing Iteration Bound, Iteration Bound of multi rate data flow graphs.	**8**	**Apply CO1**
Module-2		
Pipelining and Parallel Processing: pipelining of FIR Digital Filters, parallel processing, Pipelining and parallel processing for low power. **Retiming:** Definition and Properties, Solving Systems of Inequalities, Retiming Techniques.	**8**	**Apply CO2**
Module-3		
Unfolding: An Algorithm for Unfolding, Properties of Unfolding, Critical path, Unfolding and Retiming, Application of Unfolding. **Folding:** Folding Transformation, Register Minimization Techniques, Register Minimization in Folded Architectures, Folding of Multirate Systems.	**8**	**Apply CO3**
Module-4		
Systolic Architecture Design: systolic array design Methodology, FIR systolic array, Selection of Scheduling Vector, Matrix-Matrix Multiplication and 2D systolic Array Design, Systolic Design for space representation containing Delays. **Fast convolution**: Cook-Toom Algorithm, Winograd Algorithm, Iterated convolution, cyclic convolution Design of fast convolution Algorithm by Inspection.	**8**	**Apply CO4**
Module-5		
Algorithmic Strength Reduction in Filters and Transforms: Parallel FIR Filters, DCT and Inverse DCT, Parallel Architecture for Rank Order Filters **Pipelined and Parallel Recursive and Adaptive Filter**: Pipeline Interleaving in Digital Filter, first order IIR digital Filter, Higher order IIR digital Filter, parallel processing for IIR filter, Combined pipelining and parallel processing for IIR Filter, Low power IIR Filter Design Using Pipelining and parallel processing, pipelined adaptive digital filter	**8**	**Apply CO5**

Course Outcomes: After completing the course, the students will be able to	
23VDEP2331.1	Illustrate the use of various DSP algorithms and addresses their representation using block diagrams, signal flow graphs and data-flow graphs
23VDEP2331.2	Use pipelining and parallel processing in design of high-speed /low power applications
23VDEP2331.3	Apply unfolding in the design of parallel architecture
23VDEP2331.4	Evaluate the use of look-ahead techniques in parallel and pipelined IIR Digital filters
23VDEP2331.5	Develop an algorithm or architecture or circuit design for DSP applications

Reference Books

1. VLSI Digital Signal Processing systems, Design and implementation, Keshab K.Parthi, Wiley 1999 .
2. Analog VLSI Signal and Information Processing, Mohammed Isamail and Terri Fiez, Mc Graw-Hill,1994
3. VLSI and Modern Signal Processing, S.Y. Kung, H.J. White House, T. Kailath, Prentice Hall, 1994
4. Design of Analog - Digital VLSI Circuits for Telecommunication and Signal Processing, Jose E. France, Yannis Tsividis, Prentice Hall, 1994
5. DSP Integrated Circuits, Lars Wanhammar, Academic Press Series in Engineering, 1st Edition.

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Total	**50 Marks**

ii) SEA: 50%

Theory Exam	5 questions to answer each of 20 Marks 2 questions from each module with internal choice Student should answer one full question from each module	20 M x 5 = **100 M reduced to 50 M**
	Total	**50 Marks**

Dept. of Electronics and Communication Engineering
Choice Based Credit System (CBCS and Outcome Based Education (OBE)

Semester: III

Course Name: Machine Learning using Python		**Course Code: 23VDPE2332**
L: T: P: J	**3 :0 :0 :0**	**CIA Marks:** 50
Credits:	**3**	**SEA Marks:** 50
Hours/Week (Total)	**3**	**SEA Duration:** 03 Hours

Pre-Requisites: Programming knowledge

Course Learning Objectives: The students will be able to

1	Introduce basic concepts of Machine Learning and Python
2	Apply the knowledge of data preprocessing and regression and solve problems
3	Apply statistical knowledge to understand and interpret the relevance of the algorithm outcome
4	Apply classification algorithms and supervised learning
5	Apply unsupervised learning and preprocessing techniques

Module-1: Introduction	**No. of Hours**	**Blooms Cognitive Levels**
Overview of Machine Learning, building intelligent machines to transform data into knowledge, three different types of machine learning, An introduction to thebasic terminology and notations, A roadmap for building machine learning systems Python libraries suitable for Machine Learning: Numerical Analysis and Data Exploration with NumPy Arrays, and Data	**8**	**Apply CO1**
Module-2: Data preprocessing and Linear Regression		
Introduction to Machine learning, building a machine learning model, Data preprocessing, data exploration, outlier treatment, imputation. Correlation analysis, Simple Linear Regression, Multiple Linear Regression. Problem solving in Python	**8**	**Apply CO2**
Module-3: Statistics for Machine Learning		
Introduction, Mean, Median and Mode, Standard Deviation, Percentiles, scatterplot, types of data, measures of centers, measures of dispersion. Problem solving in Python	**8**	**Apply CO3**
Module-4: Classification models		
Introduction to Classification models, Logistic Regression, K-nearest neighbors (KNN), and Linear Discriminant Analysis (LDA). Classification problems on prediction using Python	**8**	**Apply CO4**
Module-5: Decision trees and SVM		
Simple decision trees, simple classification tree. Ensemble techniques-Bagging, Random Forest, Boosting Support Vector Machines – Introduction, Support Vector classifiers,Creating SVM model in Python	**8**	**Apply CO5**

Course Outcomes: After completing the course, the students will be able to	
23VDPE2332.1	Introduce basic concepts of Machine Learning and Python
23VDPE2332.2	Apply the knowledge of data preprocessing and regression and solve problems
23VDPE2332.3	Apply statistical knowledge to understand and interpret the relevance of the algorithm outcome
23VDPE2332.4	Apply classification algorithms and supervised learning
23VDPE2332.5	Apply unsupervised learning and preprocessing techniques
23VDPE2332.6	Able to apply the knowledge of machine learning to real-life scenarios.

Reference Books

1. Chris Albon, Machine Learning with Python Cookbook, O'Reilly, 2018.
2. E.Alpaydin, Introduction to Machine Learning, Prentice-Hall of India, 2010

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M. Tech. (VLSI Design & Embedded System)
Choice Based Credit System (CBCS and Outcome Based Education (OBE)

Semester: III

Course Name: Synthesis and Optimization of Digital Circuits **Course Code: 23VDEP2333**

L: T: P: J	**3:0:0:0**	**CIA Marks: 50**
Credits:	**3**	**SEA Marks: 50**
Hours/Week (Total)	**3**	**SEA Duration:** 03 Hours

Course Learning Objectives: The students will be able to

1	Understand the need for optimization and dimensions of optimization for digital circuits.
2	Learn basic optimization techniques used in circuits design.
3	Get the knowledge of advanced tools and techniques in digital systems design like Hardware Modelling and Compilation Techniques.
4	Apply Logic-Level synthesis and optimization techniques for combinational and sequential circuits.
5	Infer concept of scheduling and resource binding for optimization

Module 1: Introduction to Synthesis, Optimization & Hardware modelling	**No. of Hours**	**Blooms cognitive Levels**
Introduction to Synthesis and optimization: Design of Microelectronics circuits, Computer aided Synthesis and Optimization. **Hardware Modelling**: Introduction, Hardware Modelling Languages, Distinctive Features of Hardware Languages, Structural Hardware Languages, Behavioural Hardware Languages, HDLs Used for Synthesis, Abstract Models, Compilation and Behavioural Optimization **Architectural Synthesis and Optimization:** Fundamental Architectural Synthesis problems, Area and Performance Estimation, Strategies for Architectural Optimization	**8**	**Apply CO1**
Module-2 Graph theory for CAD for VLSI		
Graphs, Combinatorial Optimization, Graph Optimization problems and Algorithms, Boolean Algebra and Applications.	**8**	**Apply CO2**
Module-3 Two level and Multiple Level Combinational Logic Optimization		
Two level Combinational Logic Optimization: Introduction, Logic Optimizations, Operations on Two level Logic Covers **Multiple Level Combinational Logic Optimization**: Introduction, Models and Transformations for Combinational Networks, The Algebraic Model, The Boolean Model	**8**	**Apply CO3**
Module-4 Sequential Logic Optimization		
Introduction, Sequential Logic Optimization using State based Models, Sequential Logic Optimization using Network Models, Implicit FSM Traversal Methods, Testability Considerations for Synchronous Circuits	**8**	**Apply CO4**
Module-5 Scheduling Algorithms and Resource Sharing and Binding		
Scheduling Algorithms: Introduction, A Model for Scheduling problems, Scheduling with Resource Constraints, scheduling without Resource Constraints, Scheduling Algorithms for Extended Sequencing Models, Scheduling Pipelined Circuits. **Resource Sharing and Binding:** Sharing and Binding for Resource dominated circuits, Sharing and Binding for General Circuits, Concurrent Binding and Scheduling, Resource sharing and Binding for Non – Scheduled Sequencing Graphs.	**8**	**Apply CO5**

Course Outcomes: After completing the course, the students will be able to	
23VDEP2333.1	Understand the process of synthesis and optimization in a top-down approach for digital circuit models using HDLs and Architecture.
23VDEP2333.2	Understand the terminologies of graph theory and its algorithms to optimize a Boolean equation
23VDEP2333.3	Apply different two level and multilevel optimization algorithms for combinational circuits.
23VDEP2333.4	Apply the different sequential circuit optimization methods using state models and network models.
23VDEP2333.5	Apply different scheduling algorithms with resource binding and without resource binding for pipelined sequential circuits and extended sequencing models.

Reference Books

1. Synthesis and Optimization of Digital Circuits, Giovanni De Micheli, Tata McGraw-Hill, 2003
2. Automatic Logic synthesis Techniques for Digital Systems, Edwars M. D, Macmillan New Electronic Series, 1992

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