B N M Institute of Technology

An Autonomous Institution under VTU. Approved by AICTE

Department: Electronics and Communication Engineering

Scheme of Teaching and Examination - Autonomous Effective from Academic year 2024-25

II Semester M. Tech (VLSI Design and Embedded Systems)

Sl. No	Course Type	Course Code	Course Title	Teaching Department	Teaching Hours /Week					Examination			
					L	T	P	J	Hours/ Week	Credits	CIA Marks	SEA Marks	Total Marks
1	PCC	24VDE221	VLSI Testing and Testability	ECE	4	-	-	-	4	4	50	50	100
2	PCI	24VDE222	Low Power VLSI Design	ECE	3	-	2	-	5	4	50	50	100
3	PCI	24VDE223	Design of Analog and Mixed Mode VLSI Circuits	ECE	3	-	2	-	5	4	50	50	100
4	PBL	24VDE224	System Verilog for Verification	ECE	2	-	2	2	6	4	50	50	100
5	PEC	24VDEP225X	24VDEP2251 Reconfigurable Computing	ECE	3	-	-	-	3	3	50	50	100
	PEC		24VDEP2252 Static Timing Analysis										
	PEC		24VDEP2253 Wearable Technology										
6	PCC	24VDE226	Project Management and Finance	ECE	3	-	-	-	3	3	50	50	100
TOTAL					18	0	6	2	26	22	300	300	600

Summer Internship to be carried out during the vacation between II & III Semester

Summer Internship - I (24VDEI235): All the students registered to II year of MTech shall have to undergo mandatory internship of 4 weeks during II semester or III semester vacation. Semester End Assessment will be conducted in III semester and the prescribed credit will be included. Internship shall be considered as a head of passing and shall be considered for the award of degree. Those, who do not take up / complete the internship shall be declared fail and shall have to complete during subsequent examination after satisfying the internship requirements. (The faculty coordinator or mentor has to monitor the students' internship progress and interact to guide them for the successful completion of the internship.)

Dept. of Electronics and Communication Engineering
M.Tech (VLSI Design and Embedded Systems)
Choice Based Credit System (CBCS and Outcome Based Education (OBE)

Semester: II

Course Name: VLSI Testing and Testability		**Course Code: 24VDE221**
L: T: P: J:	**4: 0: 0: 0**	**CIE Marks: 50**
Credits:	**4**	**SEE Marks: 50**
Hours/Week:	**4 (50)**	**SEE Duration: 03 Hours**

Pre-Requisites: Basic courses on Digital circuit design, Knowledge about simulation and Logic Design.

Course Learning Objectives: The students will be able to

1	Learn various types of faults and fault modelling
2	Comprehend the need for testing and testable design of digital circuits
3	Illustrate methods and algorithms for testing digital combinatorial networks and test pattern generation
4	Exemplify methods for testing sequential circuits and memory testing
5	Inferring testing methods using Boundary scan, Built-in self-test and other advanced topics in digital circuit design

Module-1: Introduction, VLSI Testing Process and Fault Models	**No. of Hours**	**Blooms Cognitive Levels**
Testing Philosophy, Role of Testing, Digital and Analog VLSI Testing, VLSI Technology Trends affecting Testing, Types of Testing, Fault Modelling: Defects, Errors and Faults, Functional Versus Structural Testing, Levels of Fault Models, Single Stuck-at Fault.	**10**	**Understand CO1**
Module-2: Logic and Fault Simulation		
Simulation for Design Verification and Test Evaluation, Modelling Circuits for Simulation, Algorithms for True-value Simulation, Algorithms for Fault Simulation, ATPG. Fault Diagnosis of Digital Circuits, Test Generation Techniques for Combinational Circuits, Detection of Multiple Faults in Combinational Logic Circuits.	**10**	**Apply CO2**
Module-3: Testability Measures		
SCOAP Controllability and Observability, High Level Testability Measures, Digital DFT and Scan Design: Ad- Hoc DFT Methods, Scan Design, Partial-Scan Design, Variations of Scan, Ad-Hoc DFT Methods.	**10**	**Apply CO3**
Module-4: Built-In Self-Test		
The Economic Case for BIST, Random Logic BIST: Definitions, BIST Process, Pattern Generation, Response Compaction, Built-In Logic Block Observers, Test-Per-Clock, Test-Per Scan BIST Systems, Circular Self-Test Path System, Memory BIST, Delay Fault BIST, Logic Built in Self-Test.	**10**	**Apply CO4**
Module-5: Boundary Scan Standard		
Motivation, System Configuration with BoundaryScan: TAP Controller and Port, Boundary Scan Test Instructions, Pin Constraints of the Standard, Boundary Scan Description Language: BDSLDescription Components, Pin Descriptions, Boundary Scan for Asynchronous Processor	**10**	**Apply CO5**

Reference Books
1. Essentials of Electronic Testing for Digital, Memory and Mixed Signal VLSI Circuits -M.L.Bushnell, V. D. Agrawal, Kluwer Academic Publishers. 2. Digital Systems and Testable Design - M. Abramovici, M.A.Breuer and A.D Friedman,Jaico Publishing House 3. Digital Circuits Testing and Testability - P.K. Lala, Academic Press

<table>
<tr><th rowspan="2">PCC</th><th rowspan="2">CIA</th><th rowspan="2">SEA</th><th colspan="3">CIA (50)</th><th rowspan="2">SEA
Conduction: 100 M
Reduced to: 50 M</th></tr>
<tr><th></th><th>I</th><th>II</th></tr>
<tr><td rowspan="5">Conduction</td><td rowspan="5">50</td><td rowspan="5">50</td><td rowspan="2">Written Test</td><td>50</td><td>50</td><td rowspan="4">Five questions with each of 20 marks (with internal choice). Student should answer one full question from each module</td></tr>
<tr><td colspan="2">Average of two tests – 25 Marks</td></tr>
<tr><td>Assignment</td><td colspan="2">15</td></tr>
<tr><td>AAT</td><td colspan="2">10</td></tr>
<tr><td colspan="3">Total – 50 marks</td><td>Total – 50 marks</td></tr>
</table>

i) CIA: 50%

IA Test: 2 IA tests - Each of 50 Marks	Average of 2 tests – scaled down to 25 M
Assignment – Two assignments – one for 10 marks and another for 5 marks	15 Marks
Additional Assessment Tools (AAT) – Oral /Online Quizzes, Presentations, Group discussions, Case studies, Term Paper, Open ended experiments, Mini industrial/social/rural Projects, Two-minute video on latest topic, Short MOOC courses, Practical Orientation on Design thinking, creativity & Innovation, Participatory & Industry integrated learning, Practical activities, Problem solving exercises, Participation in seminars/academic events/symposia and any other activity	10 Marks
Total	**50 Marks**

ii) SEA: 50%

Theory Exam	5 questions to answer each of 20 Marks 2 questions from each module with internal choice Student should answer one full question from each module	20 M x 5 = **100 M** **reduced to 50 M**
	Total	**50 Marks**

Dept. of Electronics and Communication Engineering
M.Tech (VLSI Design and Embedded Systems)
Choice Based Credit System (CBCS and Outcome Based Education (OBE))

Semester: II

Course Name: Low Power VLSI Design		**Course Code: 24VDE222**
L: T: P: J	**3: 0 :2: 0**	**CIA Marks:** 50
Credits:	**4**	**SEA Marks:** 50
Hours/Week (Total)	**5**	**SEA Duration:** 03 Hours

Pre-Requisites: CMOS Logic Design, Power and energy relations in a capacitor, MOSFET Characteristics, Short channel effects in a MOSFET, Combinational and Sequential circuits.

Course Learning Objectives: The students will be able to

1	Understand the state-of-the-art approaches to power estimation and reduction.
2	Describe the various power reduction and the power estimation methods.
3	Explain power dissipation at all layers of design hierarchy from technology, circuit, logic, architecture and system.
4	Practice the low power techniques using current generation design style and process technology.
5	Understand the advanced techniques in low power design methods.

Module-1: Introduction to Low power Design	**No. of Hours**	**Blooms Cognitive Levels**
Introduction: Need for low power VLSI chips, charging and discharging capacitance, short circuit current in CMOS leakage current, static current, basic principles of low power design, low power figure of merits. **Simulation power analysis**: SPICE circuit simulation, discrete transistor modeling and analysis, gate level logic simulation, architecture level analysis, data correlation analysis in DSP systems, Monte Carlo simulation.	**10**	**Apply CO1**
Module-2: Power Estimation methods		
Probabilistic power analysis: Random logic signals, probability & frequency, probabilistic power analysis techniques, signal entropy. **Circuit**: Transistor and gate sizing, equivalent pin ordering, network restructuring and reorganization, special latches and flip flops, low power digital cell library, adjustable device threshold voltage.	**10**	**Apply CO2**
Module-3: Low power Design at Logic Level and Clock distribution		
Logic: Gate reorganization, signal gating, logic encoding, state machine encoding, pre-computation logic. **Low power Clock Distribution:** Power dissipation in clock distribution, single driver Vs distributed buffers, Zero skew Vs tolerable skew, chip & package co design of clock network.	**10**	**Apply CO3**
Module-4: Low power Design at Architecture/System Level		
Low power Architecture & Systems: Power & performance management, switching activity reduction, parallel architecture with voltage reduction, flow graph transformation. **Low power arithmetic components**: Introduction, circuit design style, adders, multipliers, division.	**10**	**Analyze CO4**
Module-5: Low power Memory Design and Algorithm level methods		
Low power memory design: Introduction, sources and reductions of power dissipation in memory subsystem, sources of power dissipation in DRAM and SRAM. **Algorithm & Architectural Level Methodologies**: Introduction, design flow, Algorithmic level analysis & optimization, Architectural level estimation & synthesis.	**10**	**Analyze CO5**

List of Experiments:

1. Design a traditional CMOS inverter schematic with 45 nm technology and plot its transfer (DC) characteristics and transient characteristics. Also, design a SC-SS (Low power) CMOS inverter schematic with 45 nm technology and plot its transfer (DC) characteristics and transient characteristics. Tabulate the readings (Delay, Power consumption, Power-Delay Product) for both the schematics and plot a comparison graph.

2. Design a traditional 2-input CMOS NAND gate schematic with 45 nm technology and plot its transfer (DC) characteristics and transient characteristics. Also, design a SC-SS (Low power) 2-input CMOS NAND gate schematic with 45 nm technology and plot its transfer (DC) characteristics and transient characteristics. Tabulate the readings (Delay, Power consumption, Power-Delay Product) for both the schematics and plot a comparison graph.

3. Design a traditional 2-input XOR gate (12T) schematics with 45 nm technology and plot its transfer (DC) characteristics and transient characteristics. Also, design a SC-SS (Low power) 2-input CMOS XOR gate schematic with 45 nm technology and plot its transfer (DC) characteristics and transient characteristics. Tabulate the readings (Delay, Power consumption, Power-Delay Product) for both the schematics and plot a comparison graph.

4. Design a traditional Half Adder schematic with 45 nm technology and plot its transient response. Also, design a SC-SS (Low power) Half Adder schematic with 45 nm technology and plot its transient response. Tabulate the readings (Delay, Power consumption, Power-Delay Product) for both the schematics and plot a comparison graph.

5. Design a traditional Full Adder schematic with 45 nm technology and plot its transient response. Also, design a SC-SS (Low power) Full Adder schematic with 45 nm technology and plot its transient response. Tabulate the readings (Delay, Power consumption, Power-Delay Product) for both the schematics and plot a comparison graph.

6. Design a traditional D Flip-Flop schematic with 45 nm technology and plot its transient response. Also, design a D Flip-Flop with self clock-gating schematic (Low power) with 45 nm technology and plot its transient response. Tabulate the readings (Delay, Power consumption, Power-Delay Product) for both the schematics and plot a comparison graph.

7. Design a 4-bit ripple carry adder schematic with 45 nm technology and plot its transient response. Also, design a 4-bit Carry save adder schematic with 45 nm technology and plot its transient response. Tabulate the readings (Delay, Power consumption, Power-Delay Product) for both the schematics and plot a comparison graph.

8. Design a basic 6T SRAM Cell schematic with 45 nm technology and plot its transient response. Also, design a 10T SRAM Cell schematic with 45 nm technology and plot plot its transient response. Tabulate the readings (Delay, Power consumption) for both the schematics and plot a comparison graph.

EDA Tools: Cadence-Virtuoso, LT Spice.

Course Outcomes: After completing the course, the students will be able to	
24VDE222.1	Identify the sources of power dissipation in CMOS circuits.
24VDE222.2	Perform power analysis using simulation-based approaches and probabilistic analysis.
24VDE222.3	Develop the optimization and trade-off techniques that involve power dissipation of digital circuits.

24VDE222.4	Apply the low power design techniques at the architecture and system level.
24VDE222.5	Analyze and optimize the low power memory design techniques and algorithm level methods.
24VDE222.6	Develop the practical design techniques and their analysis at various levels of design abstraction and analyze how these are being captured in the latest design automation environments.

Reference Books

1. Practical Low Power Digital VLSI Design, Gary K. Yeap, Kluwer Academic Publishers, ISBN 978-1- 4613-7778-8, 2002.
2. Low Power Design Methodologies, Jan M. Rabaey and Massoud Pedram, Kluwer Academic Publishers, 5th reprint, 2010.
3. Low-Power CMOS VLSI Circuit Design Kaushik Roy and Sharat Prasad, John Wiley, 2000.
4. Low power digital CMOS design A. P. Chandrasekaran and W. Broadersen Kluwer academic,1995.
5. Low-Power VLSI Circuits and Systems, Ajit Pal, Springer publications, 2015.

Marks Distribution for Assessment:

<table>
<tr><th rowspan="2">PCI</th><th rowspan="2">CIA</th><th rowspan="2">SEA</th><th colspan="3">CIA (50)</th><th rowspan="2">SEA
Conduction: 100 M
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<tr><td>Practical</td><td colspan="2">Weekly Assessment – 10 Marks
IA test – 15 Marks
(IA test to be conducted for 50 M and scaled down to 15M)</td></tr>
<tr><td colspan="4">Total – 50 Marks</td><td>Total – 50 Marks</td></tr>
</table>

i) CIA: 50%

Theory	**IA Test** (Theory): 2 IA tests - each of 50 Marks – Average of 2 tests scaled down to 15 Marks **Assignment**: 2 Assignments – each of 10 marks	25 Marks
Lab	**Weekly Assessment** – 10 Marks **Practical test (1)** - 15 marks	25 Marks
	Total	**50 Marks**

ii) SEA: 50%

Question Paper:

Theory Exam	5 questions to answer, each of 20 Marks 2 questions from each module with internal choice Student should answer one full question from each module	20 M x 5 = **100 M** **Reduced to 50 M**
	Total	**50 Marks**

Dept. of Electronics and Communication Engineering
M.Tech (VLSI Design and Embedded Systems)
Choice Based Credit System (CBCS and Outcome Based Education (OBE)

Semester: II

Course Name: DESIGN OF ANALOG AND MIXED MODE VLSI CIRCUITS
Course Code: 24VDE223

L: T: P: J	**3 : 0 : 2 : 0**	**CIA Marks:** 50
Credits:	**4**	**SEA Marks:** 50
Hours/Week (Total)	**5(50)**	**SEA Duration:** 03 Hours

Pre-Requisites: General considerations of MOS devices, MOS I/V Characteristics, second order effects, Basics to Amplifiers, Introduction to concepts of current mirrors and Op-Amp,Op-amp Parameters and Introduction to DAC and ADC.

Course Learning Objectives: The students will be able to

1	Describe the basic physics and operation of MOS devices
2	Exemplify single-stage and differential amplifiers and current mirrors
3	Describe operational amplifiers
4	Learn the design of phase-locked-loops
5	Know the role of Data converters in an ever-increasing digital world.

Module-1: Single stage Amplifier	**No. of Hours**	**Blooms Cognitive Levels**
Single stage Amplifier: Common Source stage, Source follower, Common-gate stage, Cascode Stage. Lab Experiment: 1 to 5	**10**	**Understand CO1**
Module-2: Differential Amplifiers		
Differential Amplifiers: Single ended and differential operation, Basic differential pair, Common mode response, Differential pair with MOS loads, Gilbert cell. Lab Experiment: 6 & 7	**10**	**Apply CO2**
Module-3: Passive and Active Current Mirrors & Operational Amplifiers (Part-1)		
Passive and Active Current Mirrors: Basiccurrent mirrors, Cascode Current mirrors, Active Current mirrors. **Operational Amplifiers (part-1):** General Considerations, OneStage OP-Amp, Two Stage OP-Amp, Gain boosting Lab Experiment: 8	**10**	**Apply CO3**
Module-4: Operational Amplifiers (part-2) & Phase Locked Loops:		
Operational Amplifiers (part-2): Common Mode Feedback, Slew rate, Power Supply Rejection. Phase Locked Loops: Simple PLL, Charge pump PLLs, Non-ideal effects in PLLs, Delay-Locked Loops.	**10**	**Apply CO4**
Module-5: Data Converter Architectures:		
Data Converter Architectures: DAC & ADC Specifications, Current Steering DAC, Charge Scaling DAC, Cyclic DAC, Pipeline DAC. Flash ADC, Pipeline ADC, Integrating ADC	**10**	**Understand CO5**

Lab Experiments:

1. Design the Common Source amplifier with Current Source Load completing the design flow for
   a. Draw the schematic and verify the following
      - DC Analysis
      - AC Analysis
      - Transient Analysis

   b. Draw the Layout and verify the DRC, check for LVS, Extract RC and back annotate the same and verify the Design.
2. Design the Common Source **amplifier with Diode connected load** completing the design flow for
   a. Draw the schematic and verify the following

- DC Analysis
- AC Analysis
- Transient Analysis

b. Draw the Layout and verify the DRC, check for LVS, Extract RC and back annotate the same and verify the Design.

3. Design the Common Source **amplifier with resistive load** completing the design flow for
   a. Draw the schematic and verify the following
      - DC Analysis
      - AC Analysis
      - Transient Analysis

   b. Draw the Layout and verify the DRC, check for LVS d. Extract RC and back annotate the same and verify the Design.
4. Design the **Common Drain** with given specifications completing the design flow for
   a. Draw the schematic and verify the following
      - DC Analysis
      - AC Analysis
      - Transient Analysis

   b. Draw the Layout and verify the DRC, check for LVS d. Extract RC and back annotate the same and verify the Design.
5. Design the **Common Gate** with given specifications completing the design flow for
   a. Draw the schematic and verify the following
      - DC Analysis
      - AC Analysis
      - Transient Analysis

   b. Draw the Layout and verify the DRC, check for LVS, Extract RC and back annotate the same and verify the Design.
6. Design the **Current Mirror** with given specifications completing the design flow for
   a. Draw the schematic and verify the following
      - DC Analysis
      - AC Analysis
      - Transient Analysis

   b. Draw the Layout and verify the DRC. Check for LVS, Extract RC and back annotate the same and verify the Design.
7. Design the **Differential Amplifier** completing the design flow for
   a. Draw the schematic and verify the following
      - DC Analysis
      - AC Analysis
      - Transient Analysis

   b. Draw the Layout and verify the DRC. Check for LVS, Extract RC and back annotate the same and verify the Design.
8. Design an **op-amp** using the **differential amplifier** with Common source and Common Drain amplifier in library, completing the design flow mentioned below:
   a. Draw the schematic and verify the following
      - DC Analysis
      - AC Analysis
      - Transient Analysis.

   b. Draw the Layout and verify the DRC, Check for LVS, Extract RC and back annotate the same and verify the Design.

Course Outcomes: After completing the course, the students will be able to	
24VDE223.1	Derive small signal model of MOSFET with second order effects and estimate the parameters for single stage CS, CG, source follower and cascade stage.
24VDE223.2	Design high-performance, stable operational amplifiers with the tradeoffs between speed, precision and power dissipation, study the behaviour of phase-locked-loopsfor the applications.
24VDE223.3	Identify the critical parameters that affect the analog and mixed-signal VLSI circuits' performance.
24VDE223.4	Perform calculations in the digital or discrete time domain, more sophisticated data converters to translate the digital data to and from inherently analog world.
24VDE223.5	Apply concepts of both Analog and digital design for VLSI Technology.
24VDE223.6	Use efficient analytical tools for quantifying the behaviour of basic circuits byinspection.

Reference Books

1. Design of Analog CMOS Integrated Circuits Behzad Razavi TMH 2007
2. CMOS Circuit Design, Layout, and Simulation R. Jacob Baker Wiley Second Edition
3. CMOS Analog Circuit Design Phillip E. Allen, Douglas R. Holberg Oxford UniversityPress Second Edition.

PCI	CIA	SEA	CIA (50)			SEA
				I	II	**Conduction: 100 M Reduced to: 50 M**
Conduction	50	50	Written Test	50	50	Five questions with each of 20 marks (with internal choice). Student should answer one full question from each module
				Average of two tests – 50 marks scaled down to 15 marks		
			Assignment	Average of 2 Assignments – 10M		
			Practical	Weekly Assessment – 10 Marks IA test – 15 Marks (IA test to be conducted for 50 M and scaled down to 15M)		
			Total – 50 Marks			**Total – 50 Marks**

i) CIA: 50%

Theory	**IA Test** (Theory): 2 IA tests - each of 50 Marks – Average of 2 tests scaled down to 15 Marks **Assignment**: 2 Assignments – each of 10 marks	25 Marks
Lab	**Weekly Assessment** – 10 Marks **Practical test (1)** - 15 marks	25 Marks
	Total	**50 Marks**

ii) SEA: 50%

Question Paper:

Theory Exam	5 questions to answer, each of 20 Marks 2 questions from each module with internal choice Student should answer one full question from each module	20 M x 5 = **100 M** **Reduced to 50 M**
	Total	**50 Marks**

Dept. of Electronics and Communication Engineering
M.Tech (VLSI Design and Embedded Systems)
Choice Based Credit System (CBCS and Outcome Based Education (OBE)

Semester: II

Course Name: System Verilog for Verification		**Course Code: 24VDE224**
L: T: P: J	**2: 0: 2: 2**	**CIA Marks:** 50
Credits:	**4**	**SEA Marks:** 50
Hours/Week (Total)	**6(50)**	**SEA Duration:** 03 Hours

Pre-Requisites: Basics understanding of combinational and sequential logic circuits, Basics of C and C++ language, Knowledge about Simulation, Verilog HDL concepts and programming

Course Learning Objectives: The students will be able to

1	Understand digital system verification using object oriented methods.
2	Learn the System Verilog language for digital system verification.
3	Create/build test benches for the basic design/methodology.
4	Use constrained random tests for verification.
5	Understand concepts of Interprocess communication and functional coverage.

Module-1: Verification Guidelines & Procedural Statements and Routines	**No. of Hours**	**Blooms Cognitive Levels**
Verification Guidelines: The verification process, basic test bench functionality, directed testing, methodology basics, constrained random stimulus, randomization, functional coverage, test bench components,layered testbench. **Connecting the test bench and design** Separating the test bench and design, The interface construct, Stimulus timing, Interface driving and sampling, System Verilog assertions. **Lab Experiment: 1 & 2**	**10**	**Apply CO1**
Module-2: Basic OOP		
Introduction, Think of Nouns, not Verbs, Your First Class, Where to Define a Class, OOP Terminology, Creating New Objects, Object Deallocation, Using Objects, Static Variables vs. Global Variables, Class Methods, Defining Methods Outside of the Class, Scoping Rules, Understanding Dynamic Objects, Public vs. Local , Building a Testbench **Lab Experiment: 3**	**10**	**Apply CO2**
Module-3: Randomization		
Introduction, Randomization in System Verilog, Constraint details, Solution probabilities, Valid constraints, In-line constraints, Random number functions, Common randomization problems, Random control, Random Number Generators. **Lab Experiment: 4 & 5**	**10**	**Apply CO3**
Module-4: Threads and Interprocess Communication		
Working with Threads, Disabling Threads, Events, Semaphores, Mailboxes **Lab Experiment: 6, 7 & 8**	**10**	**Apply CO4**
Module-5: Functional Coverage		
Coverage types, Coverage strategies, Simple coverage example, Anatomy of Cover group and Triggering a Cover group, Data sampling, Cross coverage, Generic Cover groups, Coverage options, Analyzing coverage data, measuring coverage statistics during simulation. **Lab Experiment: 9 & 10**	**10**	**Apply CO5**

Lab Experiments:

1. Develop a System Verilog code to demonstrate two-state and four-state data types.
2. Develop a System Verilog code to demonstrate push_front, pop_front, with respect to Queues.
3. Demonstrate Full adder using System Verilog with 'Interface' construct.
4. Develop a System Verilog code to demonstrate classes.
5. Write a program to create an array (Fixed Array and Dynamic Array) of objects in System Verilog.
6. Write a program to demonstrate the difference between 'rand' and 'randc'.
7. Write a program to demonstrate weighted random distribution with dist.

8. Demonstrate Interprocess Communication in System Verilog.
9. Demonstrate 4-bit adder with the verification environment
10. Write a System Verilog code to declare explicit Bins.

Projects:

1. Verification of Vedic Multiplier using System Verilog.
2. Verification of Convolutional Encoder and Viterbi Decoder using System Verilog.
3. Verification of Signed integer divider using System Verilog.
4. Verification of Wallace Tree Multiplier using System Verilog.
5. Verification of Fixed Point Arithmetic Operations using System Verilog.

Course Outcomes: After completing the course, the students will be able to	
24VDE224.1	Understand the verification guideline in test benches for moderately complex digital circuits.
24VDE224.2	Demonstrate the skill on writing test-benches for design digital systems and connecting them with the design.
24VDE224.3	Apply OOPs concepts to verify and analyze the complete system.
24VDE224.4	Apply constrained random tests benches using System Verilog
24VDE224.5	Demonstrate Threads and Interprocess communication in System Verilog.
24VDE224.6	Apply functional coverage strategies for analyzing coverage of data and coverage statistics.

Reference Books

1. Chris Spear, 'System Verilog for Verification – A guide to learning the Test bench language features', Springer Publications, 2nd Edition, 2010.
2. Stuart Sutherland, Simon Davidmann, Peter Flake, "System Verilog for DesignA guide to using system verilog for Hardware design and modeling", Springer Pulications, 2nd Edition, 2006.
3. Stuart Sutherland, Simon Davidmann, Peter Flake, "System Verilog for Design Second Edition: A Guide to Using System Verilog for Hardware Design and Modeling", Springer Science & Business Media, 15-Sep-2006.
4. Janick Bergeron, "Writing Testbenches Using SystemVerilog", 1st Edition, Springer Publications, 2006.
5. Janick Bergeron, Eduard Cerny, Alan Hunter, and Andy Nightingale, "Verification Methodology Manual for SystemVerilog", Springer Pulications, 2006.

<table>
<tr><th>PBL</th><th>CIA</th><th>SEA</th><th colspan="3">CIA (50)</th><th>SEA
Conduction: 100 M
Reduced to: 50 M</th></tr>
<tr><td rowspan="5">Conduction</td><td rowspan="5">50</td><td rowspan="5">50</td><td rowspan="3">Theory</td><td>I IA</td><td>II IA</td><td rowspan="4">Project
Assessed for 100 marks
reduced to 50 Marks</td></tr>
<tr><td>25</td><td>25</td></tr>
<tr><td colspan="2">Average of 2 tests – 25 M</td></tr>
<tr><td>Practical</td><td colspan="2">Weekly Assessment (Record/Project) – 10 Marks
Lab IA test – 15 Marks</td></tr>
<tr><td colspan="3">Total – 50 Marks</td><td>Total – 50 Marks</td></tr>
</table>

i) CIA: 50%

Theory - 2 IA tests - Each of 25 Marks	25 Marks
Practical **Weekly Assessment** - Lab record/Project – 10 Marks **Lab IA test –** 15 Marks	25 Marks
Total	**50 Marks**

ii) SEA : 50%

Project	Write up – 10 Marks Project report – 25 Marks Presentation & Demonstration - 50 Marks Viva-Voce – 15 Marks	100 Marks Reduced to 50 Marks
	Total	**50 Marks**

Dept. of Electronics and Communication Engineering
M. Tech (VLSI Design and Embedded Systems)
Choice Based Credit System (CBCS and Outcome Based Education (OBE) Semester: II

Course Name: Wearable Technology		**Course Code: 24VDEP2253**
L: T: P: J	**3: 0: 0 :0**	**CIE Marks: 50**
Credits:	**3**	**SEE Marks: 50**
Hours/Week	**3**	**SEE Duration: 03 Hours**

Pre-Requisites: Embedded Systems and Sensors

Course Learning Objectives: The students will be able to

1	To provide a brief overview of the wearable technology, need for development of wearable devices, and its impact on social life.
2	Discuss the applications of various wearable inertial sensors for biomedical applications.
3	Discuss the design and development of various wearable sensors and monitoring devices for use in healthcare applications.
4	Familiar with various wearable locomotive sensors as assistive devices for tracking and navigation.
5	To understand biochemical sensors for wearables and their applications.

Module-1: Fundamental and Social Aspects of Wearable Technologies	**No. of Hours**	**Blooms cognitive Levels**
World of Wearables, Role of Wearables, Data-information-knowledge-value paradigm, The ecosystem enabling digital life, Attributes of wearables, Taxonomy for wearables, Advancements in wearables, Textiles and clothing: The meta-wearable, Challenges and opportunities, The future of wearables: Defining the research roadmap.	**8**	**Understand CO1**
Module-2: Wearable Sensors and its Applications		
Wearable Inertial Sensors - Accelerometers, Gyroscopic sensors and Magnetic sensors; Ground Force Sensors and Insole Sensors, In-Shoe Force and Pressure Measurement, Force Sensor for Sleep Condition and Respiration on the Bed, Modality of Measurement- Wearable Inertial Sensors, Invisible Sensors, Applications: Fall Risk Assessment, Fall Detection and Gait Analysis, Physical Activity monitoring: Human Kinetics, Cardiac Activity, Energy Expenditure measurement: Pedometers, Actigraphs, Recovery	**8**	**Understand CO2**
Module-3: Medical Applications of Wearable Technologies		
Wearable ECG devices: Basics of ECG and its design, Electrodes and the Electrode–Skin Interface; Wearable EEG devices: Principle and origin of EEG, Basic Measurement set-up, electrodes and instrumentation; Wearable EMG devices: EMG/ SEMG Signals, EMG Measurement – wearable surface electrodes, SEMG Signal Conditioning, Applications.	**8**	**Apply CO3**
Module-4: Wearable Assistive Devices for the Blind and Flexible Sensors		
Wearable Assistive Devices for the Blind - Hearing and Touch sensation, Assistive Devices for Fingers and Hands, Assistive Devices for wrist, forearm and feet, vests and belts, head-mounted devices. Inkjet-Printed Sensors on Flexible Substrates: Introduction, Required Physical Properties of the Printable Ink, Materials for Printed Sensors, Conducting Materials, Semiconducting Materials, Dielectric Materials, Substrates for Flexible Sensors, Polymer-Based Substrates, Paper-Based Substrates, Textile-Based Substrates, Adhesion of Printable Ink with Substrate, Inkjet-Printed Sensors for Health care, Advantage, Limitation and Future Scope of Inkjet Printing Technology for Printed Sensors.	**8**	**Apply CO4**
Module-5: Wearable Biochemical and Gas Sensors		

Chemical Substances: Gas and Odor, Introduction, Human Odor-Based Sensors, Glucose, Introduction, Glucose Sensors, Noninvasive Glucose Monitoring Devices, GlucoWatch® G2 Biographer, GlucoTrackTM; Pulse oximeter, Portable Pulse Oximeters, wearable pulse oximeter; Wearable capnometer for monitoring of expired carbon dioxide. Textile based sensors	**8**	**Apply CO5**

Course Outcomes: After completing the course, the students will be able to	
24VDEP2253.1	To identify and understand the need for development of wearable devices and its influence on various sectors.
24VDEP2253.2	To understand various wearable inertial sensors for biomedical applications
24VDEP2253.3	To comprehend the design and development of various wearable technologies for use in healthcare applications
24VDEP2253.4	To realize the role of wearable locomotive sensors as assistive devices for tracking and navigation.
24VDEP2253.5	To Design and develop various wearable devices for detection of biochemical parameters.

Reference Books

1. Edward Sazonov, Michael R Neuman, "Wearable Sensors: Fundamentals, Implementationand Applications" Elsevier, 2nd Edition 2020.
2. "Seamless Healthcare Monitoring", Toshiyo Tamura and Wenxi Chen, Springer 2018.
3. "Wearable and Autonomous Biomedical Devices and Systems for Smart Environment", byAimé Lay-Ekuakille and Subhas Chandra Mukhopadhyay, Springer 2010.
4. Subhas C. Mukhopadhyay, "Wearable Electronics Sensors-For Safe and Healthy Living", Springer International Publishing, 2015.
   "Environmental, Chemical and Medical Sensors", by Shantanu Bhattacharya, A K Agarwal,Nripen Chanda, Ashok Pandey and Ashis Kumar Sen, Springer Nature Singapore Pte Ltd. 2018.

PCC	**CIA**	**SEA**	**CIA (50)**			**SEA Conduction: 100 M Reduced to: 50 M**
				I	II	
Conduction	50	50	Written Test	50	50	Five questions with each of 20 marks (with internal choice). Student should answer one full question from each module
				Average of two tests – 25 Marks		
			Assignment	15		
			AAT	10		
			Total – 50 marks			**Total – 50 marks**

i) CIA: 50%

IA Test: 2 IA tests - Each of 50 Marks	Average of 2 tests – scaled down to 25 M
Assignment – Two assignments – one for 10 marks and another for 5marks	15 Marks
Additional Assessment Tools (AAT) – Oral /Online Quizzes, Presentations, Group discussions, Case studies, Term Paper, Open ended experiments, Mini industrial/social/rural Projects, Two-minute video on latest topic, Short MOOC courses, Practical Orientation on Design thinking, creativity & Innovation, Participatory & Industry integrated learning, Practical activities, Problem solving exercises, Participation in seminars/academic events/symposia and any other activity	10 Marks
Total	**50 Marks**

ii) SEA: 50%

Theory Exam	5 questions to answer each of 20 Marks 2 questions from each module with internal choice Student should answer one full question from each module	20 M x 5 = **100 M reduced to 50 M**
	Total	**50 Marks**

Dept. of Electronics and Communication Engineering
M. Tech (VLSI Design and Embedded Systems)
Choice Based Credit System (CBCS and Outcome Based Education (OBE)
Semester: II

Course Name: Project Management and Finance		**Course Code: 24VDE226**
L: T: P: J:	**3: 0: 0: 0**	**CIE Marks: 50**
Credits:	**3**	**SEE Marks: 50**
Hours/Week (Total):	**3 (40)**	**SEE Duration: 03 Hours**

Pre-Requisites: Basics of management and Management functions

Course Learning Objectives: The students will be able to

1	Understand Project and its classification
2	Understand Project identification and Selection
3	To design project using various tools
4	Understand the basic concepts of financial management and financial system.
5	Understand the sources of financing and make investment decisions.

Module-1: Introduction to Project Management	**No. of Hours**	**Blooms Cognitive Levels**
A Project. Search for a Business idea: Introduction, Choosing an Idea, Selection of product, The Adoption process, Product Innovation, Product Planning and Development Strategy, Product Planning and Development Process. Concepts of Projects and Classification: Introduction, Meaning of Projects, Characteristics of a Project, Project Levels, Project Classification, Aspects of a Project.	**08**	**Understand CO1**
Module-2: Project Cycle		
The project Cycle, Features and Phases of Project management, Project Management Processes. Project Identification: Feasibility Report, Project Feasibility Analysis. Project Formulation: Meaning, Steps in Project formulation, Sequential Stages of Project Formulation, Project Evaluation.	**08**	**Understand CO2**
Module-3: Project Design and Network Analysis		
Project Design and Network Analysis: Introduction, Importance of Network Analysis, Origin of PERT and CPM, Network, Network Techniques, Need for Network Techniques, Steps in PERT, CPM, Advantages, Limitations and Differences. Project design software tools.	**08**	**Apply CO3**
Module-4: Introduction to Financial Management		
Meaning and objectives of Financial Management, changing role of financemanagers. Interface of Financial Management with other functional areas. Indian Financial System: Financial markets, Financial Instruments, Financial institutions and financial services. Emerging issues in Financial Management: Risk Management, Behavioral Finance, Financial Engineering, Derivatives (Theory).	**08**	**Analyze CO4**
Module-5: Sources of Financing and Investment Decisions		
Shares, Debentures, Term loans, Lease financing, Hybrid financing, Venture Capital, Angel investing and private equity, Warrants and convertibles (Theory Only). Capital budgeting process, Investment evaluation techniques – Net present value, Internal rate of return, modified internal rate of return, Profitability index, Payback period, discounted payback period, accounting rate of return problem, Risk analysis in capital budgeting	**08**	**Understand CO5**

Course Outcomes: After completing the course, the students will be able to	
24VDE226.1	Define the Project and its classification
24VDE226.2	Explain steps in Project identification and Selection
24VDE226.3	Design projects using various tools network tools
24VDE226.4	Explain the basic concepts of financial management and financial system.
24VDE226.5	Explain the sources of financing and make investment decisions.

Reference Books

1. Essentials of Management: An International, Innovation and Leadership perspectiveby Harold Koontz, Heinz Weihrich McGraw Hill Education, 10th Edition 2016. ISBN- 978-93-392-2286-4.
2. Avery N. Goldstein, Patent Law for Scientists and Engineers, Taylor & Francis /1st Edition/ 2005
3. Dynamics of Entrepreneurial Development and Management by Vasant Desai. HPH 2007, ISBN: 978-81-8488-801-2.
4. Professional Programme Intellectual Property Rights, Law and Practice, The Instituteof Company Secretaries of India, Statutory Body Under an Act of Parliament, September 2013. Study Material (For the topic Intellectual Property under module 4 and 5)
5. Ganguli Prabuddha, Intellectual Property Rights--Unleashing the Knowledge Economy, Tata McGrawHill (2001).
6. Financial Management by Prasanna Chandra, TMH 9/e.
7. Financial Management: A Strategic Perspective Nikhil Chandra Shil & Bhagaban Das, Sage Publications 1/e, 2016.
8. Financial Management by Khan M. Y.& Jain P. K, TMH 7/e.

Marks Distribution for Assessment:

<table>
<tr><th rowspan="2">PCC</th><th rowspan="2">CIA</th><th rowspan="2">SEA</th><th colspan="3">CIA (50)</th><th rowspan="2">SEA
Conduction: 100 M
Reduced to: 50 M</th></tr>
<tr><th></th><th>I</th><th>II</th></tr>
<tr><td rowspan="5">Conduction</td><td rowspan="5">50</td><td rowspan="5">50</td><td rowspan="2">Written Test</td><td>50</td><td>50</td><td rowspan="4">Five questions with each of 20 marks (with internal choice). Student should answer one full question from each module</td></tr>
<tr><td colspan="2">Average of two tests – 25 Marks</td></tr>
<tr><td>Assignment</td><td colspan="2">15</td></tr>
<tr><td>AAT</td><td colspan="2">10</td></tr>
<tr><td colspan="3">Total – 50 marks</td><td>Total – 50 marks</td></tr>
</table>

i) CIA: 50%

IA Test: 2 IA tests - Each of 50 Marks	Average of 2 tests – scaled down to 25 M
Assignment – Two assignments – one for 10 marks and another for 5 marks	15 Marks
Additional Assessment Tools (AAT) – Oral /Online Quizzes, Presentations, Group discussions, Case studies, Term Paper, Open ended experiments, Mini industrial/social/rural Projects, Two-minute video on latest topic, Short MOOC courses, Practical Orientation on Design thinking, creativity & Innovation, Participatory & Industry integrated learning, Practical activities, Problem solving exercises, Participation in seminars/academic events/symposia and any other activity	10 Marks
Total	**50 Marks**

ii) SEA : 50%

Theory Exam	5 questions to answer each of 20 Marks 2 questions from each module with internal choice Student should answer one full question from each module	20 M x 5 = **100 M** **reduced to 50 M**
	Total	**50 Marks**