B N M Institute of Technology

An Autonomous Institution under VTU Approved by AICTE

Department: Electronics and Communication Engineering

Scheme of Teaching and Examination-Autonomous Effective from Academic year 2025-26

I Semester M. Tech (VLSI Design and Embedded Systems)

Sl. No.	Course Type	Course Code	Course Title	Teaching Department	Teaching Hours/Week				Hours/ Week	Examination			
					L	T	P	J		Credits	CIA Marks	SEA Marks	Total Marks
1	PCC	25VDE211	Custom IC Design	ECE	4	-	-	-	4	4	50	50	100
2	PCL	25VDE212	QNX-based Embedded RTOS Design	ECE	2	-	4	-	6	4	50	50	100
3	PCI	25VDE213	Modern CMOS Circuit Design	ECE	3	-	2	-	5	4	50	50	100
4	PBL	25VDE214	System Verilog for Design and Verification	ECE	2	-	2	2	6	4	50	50	100
5	PEC	25VDEP215X	25VDEP2151 Hybrid AI models for Power-Efficient VLSI System	ECE	3	-	0	-	3	3	50	50	100
	PEC		25VDEP2152 Memory design for Low Power VLSI System.										
	PEC		25VDEP2153 Power semiconductor devices and Technology										
	PEC		25VDEP2154 Computer Aided Design of VLSI Circuits										
6	PCC	25VDE216	Research Methodology & IPR	ECE	3	-	-	-	3	3	50	50	100
TOTAL					17	0	8	2	27	22	300	300	600

L-Theory lecture, T–Tutorial, P–Practical, J–Project, NCMC-Non-Credit Mandatory Course
CIA: Continuous Internal Assessment, SEA: Semester End Assessment

Note: PCC: Professional Core Course, **HSS:** Humanity and Social Science & Management Courses, **PCI:** Professional Core Integrated, **PCL:** Professional course with Lab
PBL: Project-Based Learning, **AEC:** Ability Enhancement Courses, **PEC:** Professional Elective, **INT:** Summer Internship, **PRJ:** Project Work

Credit definition: 1 hour Lecture (L) per week = 1 Credit	2 hours Tutorial (T)per week = 1 Credit
2 hours Practical/Drawing(P) per week=1Credit	2 hours Project Component(J) per week=1Credit
(a) 4 Credit courses are to be designed for 50 hours of the Teaching–Learning process.	(b)3 Credit courses are to be designed for 40-hour teaching–learning process.
(c) 2 Credit courses are to be designedfor25hoursTeaching–Learning process	(d)1Credit course are to be designed for12-15hoursTeaching–Learning process

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B.N.M. Institute of Technology

An Autonomous Institution under VTU

Dept. of Electronics and Communication Engineering

M. Tech (VLSI Design and Embedded Systems)

Semester: I

Course Name: Custom IC DESIGN		**Course Code: 25VDE211**
L: T: P: J	**4: 0: 0: 0**	**CIA Marks:** 50
Credits:	**4**	**SEA Marks:** 50
Hours	**50**	**SEA Duration:** 03 Hours

Pre-Requisites: A Brief History of MOS Transistors, Theory and Fundamentals of Integrated Circuits, Logic Design, Basic of delay calculation and storage elements

Course Learning Objectives: The students will be able to

1	Explore the concepts of Custom IC design flow and CMOS logic cells
2	Understand the Custom IC Library Design and Programmable ASIC logic cells
3	Explore the basics of Physical Design techniques in Custom IC Design
4	Present the overview of routing techniques in Custom IC Design
5	Understand the basics of CHIPLETS

Module-1: Introduction to Custom IC Design	**No. of Hours**	**Blooms Cognitive Levels**
Types of ASICs: Full Custom ASIC, Semi- custom based ASICS, Standard Cell based ASIC, Gate array-based ASIC, Channeled gate array, Channel less gate array, Structured gate array, Programmable logic devices, FPGA, ASIC Design flow. **CMOS Logic:** Data path Logic Cells: Data Path Elements, Adders: Carry skip, Carry bypass, Carry save, Carry select, Conditional sum, Multiplier (Booth encoding), Data path Operators, I/O cells, Cell Compilers.	**10**	**Apply CO1**
Module-2: ASIC Library Design and Programmable ASIC Logic Cells		
Logical Effort: Predicting delay, Logical area and logical efficiency, Logical paths, Multistage cells, optimum delay, optimum number of stages. Library-cell design. **Programmable ASIC Logic Cells:** MUX as Boolean function generators, Shannon's expansion theorem, Actel ACT: ACT 1, ACT 2 and ACT 3 Logic Modules, Xilinx LCA: XC3000 CLB, Altera FLEX and MAX, Programmable ASIC I/O Cells: Xilinx and Altera I/O Block.	**10**	**Apply CO2**
Module-3: ASIC Physical Design: Partitioning, Floor Planning and Placement		
ASIC Construction: Physical Design, CAD Tools System partitioning, Estimating ASIC size. **Partitioning:** Goals and objectives, Constructive Partitioning, Iterative Partitioning Improvement, KL, FM and Look Ahead algorithms. **Floor planning and placement:** Goals and objectives, Measurement of delay in Floor planning, Floor planning tools, Channel definition, I/O and Power planning and Clock planning. **Placement:** Goals and Objectives, Min-cut Placement algorithm, Iterative Placement Improvement, Time driven placement methods, Physical Design Flow.	**10**	**Apply CO3**
Module-4: ASIC Physical Design: Routing Techniques		
Global Routing: Goals and objectives, Global Routing Methods, Global routing between blocks, Back annotation. **Detailed Routing:** Goals and objectives, Measurement of Channel Density, Left-Edge Algorithm, Area-Routing Algorithms, Multilevel routing, Timing –Driven detailed routing, Final routing steps, Special Routing, Circuit extraction and DRC.	**10**	**Apply CO4**

Module-5: Introduction to CHIPLETS		
Introduction to Chiplet technology, Commercial Challenges: Business and Technical, Interface Challenges, D2D Interface Types: Serial vs Parallel, Proprietary vs Open D2D Stnadards , Packaging Innovations for Chiplets, Chiplet Security Challenges: Proving and Securing Authenticity, Silicon-Based Countermeasures, Supply Chain Security & Provisioning.	**10**	**Understand CO5**

Course Outcomes: After completing the course, the students will be able to	
25VDE211.1	Design the data path elements for ASIC cell libraries and understand the concepts of ASIC design methodology
25VDE211.2	Design the Mux-based logic cells and compute the Logical effort of a single stage network and Multistage network
25VDE211.3	Apply the concepts of Partitioning, Floor planning, and Placement techniques in Custom IC Design
25VDE211.4	Apply the concepts of Global and Detailed routing techniques in Custom IC Design
25VDE211.5	Explore the various opportunities and challenges in the area of CHIPLETS
25VDE211.6	Design and implement a Custom IC for a specific application.

Reference Books

1. Application - Specific Integrated Circuits, Michael John Sebastian Smith Addison- Wesley Professional, 2015.
2. CMOS VLSI Design: A Circuits and Systems Perspective Neil H.E. Weste, David Harris,and Ayan Banerjee, Addison Wesley/ Pearson education 3rd edition, 2011.
3. VLSI Design: A Practical Guide for FPGA and ASIC Implementations, Vikram Arkalgud Chandrasetty, Springer, ISBN: 978-1-4614-1119-2. 2011.
4. An ASIC Low Power Primer, Rakesh Chadha, Bhasker J Springer, ISBN: 978-14614-4270-7.
5. Heterogeneous Integration-CHIPLETS, White Paper, https://www.gsaglobal.org/wp-content/uploads/2023/02/2022-IPIG-Heterogenous-Integration-Chiplets-White-Paper-Final-v4.pdf, 2022.
6. The March Towards Chiplets, Ed Sperling and Karen Heyman, Semiconductor Engineering December 15, 2022. https://semiengineering.com/the-march-toward-chiplets/.

Marks Distribution for Assessment:

<table>
<tr><th rowspan="2">PCC</th><th rowspan="2">CIA</th><th rowspan="2">SEA</th><th colspan="3">CIA (50)</th><th rowspan="2">SEA
Conduction: 100 M
Reduced to: 50 M</th></tr>
<tr><th></th><th>I</th><th>II</th></tr>
<tr><td rowspan="5">Conduction</td><td rowspan="5">50</td><td rowspan="5">50</td><td rowspan="2">Written Test</td><td>50</td><td>50</td><td rowspan="4">Five questions with each of 20 marks (with internal choice). Student should answer one full question from each module</td></tr>
<tr><td colspan="2">Average of two tests – 25 Marks</td></tr>
<tr><td>Assignment</td><td colspan="2">15</td></tr>
<tr><td>AAT</td><td colspan="2">10</td></tr>
<tr><td colspan="3">Total – 50 marks</td><td>Total – 50 marks</td></tr>
</table>

B.N.M. Institute of Technology

An Autonomous Institution under VTU

Dept. of Electronics and Communication Engineering

M. Tech (VLSI Design and Embedded Systems)

SEMESTER – I

Course Name: QNX based Embedded RTOS Design		**Code:** 25VDE212
L: T:P: J	**2:0:4:0**	**CIA Marks:** 50
Credits:	4	**SEA Marks:** 50
Hours	50	**SEA Duration:** 03 Hours

Course Learning Objectives:

This course will enable students to

- Understand the Architecture of QNX Neutrino RTOS and Develop Real-Time Applications
- Understand the working of QNX Development Tools (Momentics IDE)
- Able to Implement Process and Thread Management
- Understand the Master Inter-Process Communication (IPC)
- Debug and Optimize Embedded Systems

Pre-Requisites: Operating Systems basics and C programming and Linux commands.

QNX Momentics Development Basics: Eclipse Basics, Targets, Projects and Source, Compiling, Exercise, Running and Debugging, Exercise and Versions.

QNX Neutrino RTOS Environment Setup

Objective: Install and configure QNX SDP, Momentics IDE, and target system (real or virtual).

Outcome: Understand development workflow in QNX.

	Number of Hours	**Bloom's Level**
Module-1		
Introduction to QNX Real Time Operating System: Architecture – Executive, Microkernel, Inter process Communication, Processes and Threads model, Timing, Interrupt Handling, Scheduling, Boot Sequence, Security.	4	**Apply (CO1)**
Laboratory Component: Process Creation and Management **Running and Debugging: Excersise** Objective: Create and run hello world example on VM Ware virtual machine or Rasp-pi board. Outcome: Print hello world on panel of QNX Momentics IDE Objective: Write a program to create and manage multiple processes. Outcome: Demonstrate use of fork(), exec(), and wait() in QNX. **Self-Study Component:** Demonstrate how to Detect the termination of a child processes.	6	**Apply (CO1, CO2)**
Module-2		
Security Policies: Introduction to the use of security policies in securing a QNX system, Process Managers: System Library, Shared Objects, OS Services, Boot Sequence and Security.	4	**Apply (CO2)**

Processes, Threads & Synchronization: Introduction, Processes: Creation and Detecting termination, Threads, Process Termination and Cleanup,		
Laboratory Component: Thread Creation and Synchronization Processes - Detecting Termination: Exercise Synchronization - Mutexes: Solution to synchronization problems using Mutex Synchronization - Conditional Variables: Program in synchronization using Conditional Variables. **Self-Study Component:** Synchronization - Atomic Operations: Simple program solutions on atomic operations	**6**	**Apply (CO2)**
Module-3		
Introduction to QNX Inter-Process Communication: Message Passing, Designing a Message Passing System (1): Pulses, Client Information Structure, How a Client Finds a Server, Multi-Part Messages. **Comparing QNX IPC Methods:** The Methods, How to Choose.	**4**	**Understand (CO3)**
Laboratory Component: **Inter-Process Communication using Message Passing:** Implement server-client IPC using MsgSend(), MsgReceive(), and MsgReply(). Programs to demonstrate IPC with pulses Programs to demonstrate IPC with multipart messages **Self-Study Component:** Assignment on Inter-Process Communication (IPC)	**6**	**Apply (CO3, CO4)**
Module-4		
QNX Inter-Process Communication: Issues Related to Priorities, Designing a Message Passing System (2): Event Delivery Shared Memory **Introduction to Hardware Programming:** Hardware I/O, Programming PCI bus devices, Handling Interrupts.	**4**	**Apply (CO4)**
Laboratory Component: Event Delivery: Program to demonstrate IPC – event delivery Shared Memory: Implement IPC using shared memory **Self-Study Component:** Handling Interrupts : Program on Interrupt handling	**6**	**Apply (CO4)**
Module-5		
Timers, Clocks and Timeouts: Introduction, Timing Architecure, Getting and Setting the System Clock, Introduction to Timers, High-Resolution Timers, Design Considerations, Kernel Timeouts. **Build a QNX Neutrino Boot/OS Image:** Introduction, Images & Buildfiles, Images & Buildfiles: Exercise option	**4**	**Apply (CO5)**

Resource Managers: Introduction, A Simple Resource Manager: Initialization and Handling read() and write().		
Laboratory Component: Timers: Program on timers Program to initialize Resource managers. Handling read() and write() - read() ***Self-Study Component:*** Implementation of Image building	**6**	**Apply (CO5)**

Course outcomes:

The students will be able to

- Understand the Architecture of QNX Neutrino RTOS and implement Real-Time Applications
- Apply the working of QNX Development Tools (Momentics IDE) on Processes, Threads & Synchronization.
- Implement the QNX Inter-Process Communication and compare QNX IPC Methods
- Apply the QNX Inter-Process Communication with Hardware Programming and Interrupt handling
- Understand the timing architecture, High-Resolution Timers, Images & Buildfiles and Resource Manager

Reference Books:

1. Operating Systems: Three easy pieces - Remzi H. Arpaci-Dusseau, Andrea C. Arpaci-Dusseau, Books, LLC, 2018
2. The Linux Programming Interface- Michael Kerrisk, No Starch Press, 2010
3. Operating Systems: Design and Implementation - Andrew S Tanenbaum, Pearson/Prentice Hall, 2006

Marks Distribution for Assessment

CIA (50)	Components	Description	Marks
	Written test	• Total Number of Test:02 • Each Theory test will be conducted for 30 marks • Average of 2 tests= 30 Marks	**30**
	Practical	• Total number of Test: 02 [Part-A (Modue-1 and 2) and Part-B (Module 3,4 and 5)] Each Lab test will be conducted for 50 marks and reduce to 10 Average of 2 tests= 10 Marks	**10**
		• Laboratory conduction is to be evaluated every week. conducted & Viva = 5 Marks Lab Record = 5 Marks	**10**
		Total CIA	**50**
SEA (50)	Practical Exam	• Students are allowed to pick one experiment from Part-A and one experiment from PART-B. Mark Distribution: Total 100 marks Part – A: 40 Marks (Procedure:6, Execution:28, Viva: 6) Part – B: 60 Marks (Procedure:9, Execution:42, Viva: 9) Scaled down to 50 marks	**50**
		Total Marks for the Course	**100**

B.N.M. Institute of Technology

An Autonomous Institution under VTU

Dept. of Electronics and Communication Engineering

M. Tech (VLSI Design and Embedded Systems)

Semester: I

Course Name: Modern CMOS Circuit Design		**Course Code: 25VDE213**
L: T: P: J	**3: 0: 2: 0**	**CIA Marks: 50**
Credits	**4**	**SEA Marks: 50**
Hours/Week (Total)	**5 (50)**	**SEA Duration: 03 Hours**

Pre-Requisites: Metal Oxide Semiconductor (MOS) Structure, Inverters, Semiconductor memory, Concept of Pass Transistor and BJTs.

Course Learning Objectives: The students will be able to

1	Explain VLSI Design Methodologies
2	Learn Static and Dynamic operation principles, analysis and design of inverter circuit.
3	Infer state of the art Semiconductors Memory circuits.
4	Outline the comprehensive coverage of Methodologies and Design practice that are used to reduce the Power Dissipation of largescale digital circuits.
5	Illustrate VLSI and ASIC design

Module-1: MOS Transistor and MOS Inverters- Static Characteristics	**No. of Hours**	**Blooms cognitive Levels**
MOS Inverters-Static Characteristics: Introduction, Resistive-Load Inverter, Inverters with n-Type MOSFET Load. CMOS Inverter. Scaling and Small-Geometry Effects. **Lab Experiment: 1**	**10**	Apply CO1
Module-2: MOS Inverters:		
Switching Characteristics and Delay-Time Definition, Calculation of Delay Times, Inverter Design with Delay Constraints, Estimation of Interconnect Parasitics, Calculation of Interconnect Delay, Switching Power Dissipation of CMOS Inverters. **Lab Experiment: 2 & 3**	**10**	Analyze CO2
Module-3: Semiconductor Memories:		
Dynamic Random Access Memory (DRAM), Static Random Access Memory (SRAM), Nonvolatile Memory, Flash Memory & Ferroelectric Random Access Memory (FRAM) **Lab Experiment: 4 & 5**	**10**	Apply CO3
Module-4: BiCMOS and Dynamic Logic Circuits		
Dynamic Logic Circuits: Basic Principles of Pass Transistor Circuits, Voltage Bootstrapping, Synchronous Dynamic Circuit Techniques, High Performance Dynamic CMOS circuits. BiCMOS Logic Circuits: Structure and Operation, Dynamic Behavior of BJTs: Basic BiCMOS Circuits: Static Behavior and BiCMOS Applications **Lab Experiment: 6 & 7**	**10**	Apply CO4
Module-5: Overview of FinFET Device Technology		
Introduction to FinFET, FinFET Devices for VLSI Circuits and Systems, A Brief History of FinFET Devices, Construction and working of FinFET, FinFET Manufacturing Technology, Bulk-FinFET Fabrication, SOI-FinFET Process Flow. **Lab Experiment: 8 to 10**	**10**	Apply CO4

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Lab Experiments

1. Draw NMOS characteristics and Determine
   i. Cut-Off Region
   ii. Ohmic or Linear Region
   iii. Saturation Region
2. a. Design an **Inverter** with given specifications, completing the design flow mentionedbelow: a. Draw the schematic and verify the following
   i. DC Analysis
   ii. Transient Analysis

   b. Draw the Layout and verify the DRC, check for LVS Extract RC and back annotate the same and verify the Design Verify & Optimize for Time, Power andArea to the given constraint
3. a. Draw **CMOS inverter with load capacitance** of 0.1pF and set the widths of inverterwith Wn=Wp, Wn = 2Wp, Wn = Wp/2 and length at selected technology. Carryout the fallowing
   i. Set the input signal to a pulse with rise time, fall time of 1ns and pulse with of10ns and time period of 20ns and plot the input voltage and output voltage of designed inverter.
   ii. From the simulation results compute tpHL, tpLH and td for all three geometricalsettings of width.
   iii. Tabulate the results of delay and find the best geometry for minimum delay forCMOS inverter

   b. Draw layout of inverter with Wp/Wn=40/20, use optimum layout methods. Verify for DRC and LVS, extract parasitic and perform post layout simulations,compare the results.
4. Design of Dynamic CMOS Logic, Y= AB + C
5. Design of Domino CMOS Logic, Y = (A+B) * C
6. Draw the schematic of 2- input CMOS NAND gate having similar delay as that of CMOS inverter computed in experiment 2. Verify the functionality of NAND gate and also find out the delay tdfor all four possible combinations of input vectors. Table the results. Increase the drive strength to 2X and 4X and tabulate the results.

   b. Draw layout of NAND with Wp/Wn=40/20, use optimum layout methods. Verify for DRC and LVS, extract parasitic and perform post layout simulations, compare the results.
7. a. Draw the schematic of Buffer using inverter and verify the simulation.

   b. Draw layout of BUFFER circuit, verify for DRC and LVS, extract parasitic and perform postlayout simulations, compare the results.
8. Draw the schematic of TRI State INVERTER and TRI State Buffer using MOSFETs and verify the simulation. Draw layout and verify for DRC and LVS, extract parasitic and perform post layout simulations, compare the results.
9. a. Draw the schematic of D-latch using inverter and verify the simulation.

   b. Draw layout of D-latch circuit, verify for DRC and LVS, extract parasitic and perform postlayout simulations, compare the results.
10. a. Draw the schematic of D FF using gates and verify the simulation.

    b. Draw Layout of D FF Verify for DRC and LVS, extract parasitic and perform post layout simulations, compare the results.

Course Outcomes: After completing the course, the students will be able to	
25VDE213.1	Apply the design concepts to MOS inverters and CMOS inverters by understanding their static characteristics. Evaluate the effects of scaling and small-geometry devices on inverter performance for optimized digital circuit design
25VDE213.2	Analyze the Switching Characteristics in Digital Integrated Circuits.
25VDE213.3	Apply concepts study memory behavior and performance.
25VDE213.4	Apply the design concepts to evaluate BiCMOS and dynamic logic circuits.
25VDE213.5	Understand the structure, working, and applications of FinFET devices in VLSI circuits. Analyze FinFET manufacturing technologies, including Bulk and SOI process flows, for modern semiconductor design
25VDE213.6	Apply design concepts to analyze MOS, CMOS, BiCMOS, dynamic logic circuits, and FinFET devices to optimize VLSI circuit erformance

Reference Books

1. Sung Mo Kang &Yosuf Leblebici, "CMOS Digital Integrated Circuits: Analysis andDesign",Tata McGraw-Hill, Third Edition.
2. FinFET Devices for VLSI Circuits and Systems, Samar K. Saha, Taylor and Francis Group, 2020.
3. Neil Weste and K. Eshragian, "Principles of CMOS VLSI Design: A System Perspective", Second Edition, Pearson Education (Asia) Pvt. Ltd. 2000.
4. Wayne, Wolf, "Modern VLSI Design: System on Silicon" Prentice Hall PTR/Pearson Education, Second Edition, 1998.
5. Douglas A Pucknell& Kamran Eshragian, "Basic VLSI Design" PHI 3rd Edition (original Edition – 1994).

Assessment Process

Professional Core with Integrated Lab (PCI) – Course with Lab

<table>
<tr><th rowspan="2">PCI</th><th rowspan="2">CIA</th><th rowspan="2">SEA</th><th colspan="3">CIA (50)</th><th rowspan="2">SEA
Conduction: 100 M
Reduced to: 50 M</th></tr>
<tr><th></th><th>I</th><th>II</th></tr>
<tr><td rowspan="5">Conduction</td><td rowspan="5">50</td><td rowspan="5">50</td><td rowspan="2">Written Test</td><td>50</td><td>50</td><td rowspan="4">Five questions with each of 20 marks (with internal choice). Student should answer one full question from each module</td></tr>
<tr><td colspan="2">Average of two tests – 50 marks scaled down to 15 marks</td></tr>
<tr><td>Assignment</td><td colspan="2">Average of 2 Assignments – 10M</td></tr>
<tr><td>Practical</td><td colspan="2">Weekly Assessment – 10 Marks
IA test – 15 Marks
(IA test to be conducted for 50 M and scaled down to 15M)</td></tr>
<tr><td colspan="5">Total – 50 Marks</td><td>Total – 50 Marks</td></tr>
</table>

B.N.M. Institute of Technology

An Autonomous Institution under VTU

Dept. of Electronics and Communication Engineering

M. Tech (VLSI Design and Embedded Systems)

Semester: I

Course Name: System Verilog for Design and Verification		**Course Code: 25VDE214**
L: T: P: J	**2: 0: 2: 2**	**CIA Marks:** 50
Credits:	**4**	**SEA Marks:** 50
Hours	**50**	**SEA Duration:** 03 Hours

Pre-Requisites: Basics understanding of combinational and sequential logic circuits, Basics of C and C++ language, Knowledge about Simulation, Verilog HDL concepts and programming

Course Learning Objectives: The students will be able to

1	Understand digital system verification using object oriented methods.
2	Learn the System Verilog language for digital system verification.
3	Create/build test benches for the basic design/methodology.
4	Use constrained random tests for verification.
5	Understand concepts of Interprocess communication and functional coverage.

Module-1: Data Types and Verification Guidelines	**No. of Hours**	**Blooms Cognitive Levels**
Data Types : Built in data types, Fixed Size Arrays, Dynamic Arrays, Queues, Associative Arrays. Array Methods, Creating New Types with typedef, Enumerated Types, Tasks, Functions, and Void Functions **Verification Guidelines:** The verification process, directed testing, constrained random stimulus, randomization, test bench components, layered testbench. **Lab Experiment:** • Develop a System Verilog code to demonstrate two-state and four-state data types. • Write a program to create an array (Fixed Array an Dynamic Array) of objects in System Verilog. Develop a System Verilog code to demonstrate push_front, pop_front, with respect to Queues.	**10**	**Apply CO1**
Module-2: Connecting the test bench and design & OOP Concepts		
Connecting the test bench and design Separating the test bench and design, The interface construct, System Verilog assertions. **OOP Concepts** Introduction, Your First Class, Where to Define a Class, OOP Terminology, Creating New Objects, Object Deallocation, Using Objects, Static Variables vs. Global Variables, Class Methods, Defining Methods Outside of the Class, Scoping Rules **Lab Experiment:** • Demonstrate Full adder using System Verilog with 'Interface' construct. • Develop a System Verilog code to demonstrate classes.	**10**	**Apply CO2**
Module-3: Randomization		

Introduction, Randomization in System Verilog, Constraint details, Solution probabilities, Valid constraints, In-line constraints, Random number functions, Common randomization problems, Random control, Random Number Generators. **Lab Experiment:** • Write a program to demonstrate the difference between 'rand' and 'randc'. • Write a program to demonstrate weighted random distribution with dist.	**10**	**Apply CO3**
Module-4: Threads and Interprocess Communication		
Working with Threads, Disabling Threads, Events, Semaphores, Mailboxes **Lab Experiment:** • Write a program to demonstrate access control using semaphore for one/multiple key. • Write a program to demonstrate Mailbox uses in interprocess communication.	**10**	**Apply CO4**
Module-5: Functional Coverage		
Coverage types, Coverage strategies, Simple coverage example, Anatomy of Cover group and Triggering a Cover group, Data sampling, Cross coverage, Generic Cover groups, Coverage options, Analyzing coverage data, measuring coverage statistics during simulation. **Lab Experiment:** • Demonstrate 4-bit adder with the verification environment • Write a System Verilog code to declare explicit Bins.	**10**	**Apply CO5**

Projects:

1. Verification of Vedic Multiplier using System Verilog.
2. Verification of Convolutional Encoder and Viterbi Decoder using System Verilog.
3. Verification of Signed integer divider using System Verilog.
4. Verification of Wallace Tree Multiplier using System Verilog.
5. Design and verify a UART with configurable baud rate using System Verilog.

Course Outcomes: After completing the course, the students will be able to	
25VDE214.1	Apply SystemVerilog features(data types, arrays, and queues) to develop digital systems and verify using directed and randomized testing.
25VDE214.2	Implement object-oriented programming, interfaces, and assertions in SystemVerilog for efficient testbench development and verification.
25VDE214.3	Use SystemVerilog's randomization constructs(constraints, control options, and random number) utilities to enhance verification efficiency and coverage.
25VDE214.4	Apply SystemVerilog constructs (threads, events, semaphores, and mailboxes) to implement concurrent verification processes.
25VDE214.5	Evaluate the effectiveness of functional coverage and interprocess synchronization techniques in complex verification scenarios.

Reference Books

1. Chris Spear, 'System Verilog for Verification – A guide to learning the Test bench language features', Springer Publications, 3rd Edition, 2012.
2. Stuart Sutherland, Simon Davidmann, Peter Flake, "System Verilog for DesignA guide to using system verilog for Hardware design and modeling", Springer Pulications, 2nd Edition, 2008.
3. Janick Bergeron, "Writing Testbenches Using SystemVerilog", 1st Edition, Springer Publications, 2010.
4. Janick Bergeron, Eduard Cerny, Alan Hunter, and Andy Nightingale, "Verification Methodology Manual for SystemVerilog", Springer Pulications, 2014.

Marks Distribution for Assessment:

<table>
<tr><th rowspan="2">PBL</th><th rowspan="2">CIA</th><th rowspan="2">SEA</th><th colspan="3">Academic Year 2023-24
CIA (50M) T-Theory; E- Execution
M-Marks</th></tr>
<tr><td></td><td>IA -1 (40M)</td><td>IA-2(40M)</td></tr>
<tr><td rowspan="3">Conduction</td><td rowspan="3">50M</td><td rowspan="3">50M</td><td>IA TEST</td><td>20(T) + 20(E)</td><td>20(T) + 20(E)</td></tr>
<tr><td>Continuous Assessment</td><td colspan="2">Weekly Assessment (Project/record) 5+5=10M</td></tr>
<tr><td>TOTAL</td><td colspan="2">40+10= 50M</td></tr>
<tr><td>SEA(Project)</td><td>-</td><td>Project assessed for 100 marks reduced to 50 marks</td><td>Conduction :100 marks Reduced to :50 marks</td><td colspan="2">• Write up - 10M
• Project report – 25M
• Presentation and Documentation - 50M
• Viva Voce – 15M</td></tr>
<tr><td></td><td></td><td></td><td>TOTAL</td><td colspan="2">50M</td></tr>
</table>

B.N.M. Institute of Technology

An Autonomous Institution under VTU

Dept. of Electronics and Communication Engineering

M. Tech (VLSI Design and Embedded Systems)

Semester: I

Course Name: Hybrid AI models for Power Efficient VLSI system		**Course Code: 25VDEP2151**
L: T: P: J	**3 :0 :0 :0**	**CIA Marks:** 50
Credits:	**3**	**SEA Marks:** 50
Hours/Week (Total)	**3**	**SEA Duration:** 03 Hours

Pre-Requisite : Basic knowledge of Digital Electronics, CMOS Design, and introductory Machine Learning

Course Learning Objectives: The students will be able to

1	To introduce and understand the fundamentals of AI and its relevance to VLSI design.
2	To explore hybrid AI models combining various AI techniques for power optimization in VLSI systems.
3	To analyze power estimation and reduction techniques using AI methodologies.
4	To provide hands-on experience with tools and frameworks applicable to AI-driven VLSI design.
5	To evaluate case studies demonstrating the application of hybrid AI models in real-world VLSI systems.

Module 1: Introduction to AI in VLSI Design	**No. of Hours**	**Blooms Cognitive Levels**
Overview of AI techniques: Machine Learning, Deep Learning, Fuzzy Logic, Genetic Algorithms, Relevance of AI in VLSI design and power optimization, Challenges in traditional VLSI design methodologies, Introduction to hybrid AI models	**8**	**Understand CO1**
Module 2: Power Estimation Techniques using AI		
Traditional power estimation methods, Machine Learning approaches for power estimation, Integration of AI models for accurate power prediction, Case studies on AI-driven power estimation	**8**	**Apply CO2**
Module 3: Hybrid AI Models for Power Optimization		
Combining AI techniques: Fuzzy Logic, Genetic Algorithms, Neural Networks, Designing hybrid models for power optimization, Simulation and analysis of hybrid models, Comparative study of hybrid vs. traditional models.	8	**Analyse CO3**
Module 4: Frameworks and Tools for AI-Driven VLSI Design		
Theoretical Foundations: Overview of AI model deployment in EDA workflows, Role of EDA tools in power modeling, synthesis, and simulation, Understanding how ML integrates into VLSI design stages (e.g., placement, routing, floor planning), Classification of AI tools: supervised vs. unsupervised in VLSI context. Introduction to tools: MATLAB/Simulink, Python-based platforms (TensorFlow, Scikit-learn, Keras) for AI model creation, EDA tools (Cadence Virtuoso, Synopsys Design Compiler) for VLSI design, Integration of AI models with design flow: input/output mapping, Tool interoperability challenges and solutions	**8**	**Apply CO4**
Module-5: Architectures in Hybrid AI-VLSI Systems		
Foundations of Hybrid AI Architectures: Overview of hybrid AI models: neuro-fuzzy, ANN-GA, RL-based architectures, Mapping AI algorithms to hardware: RTL-aware architecture planning, Trade-offs in accuracy, latency, power, and area for AI hardware integration. Low-Power Hardware Design Techniques for AI Systems: Power-aware logic synthesis and voltage scaling for AI cores, AI-based clock and power gating in logic blocks, Interconnect and memory hierarchy optimization for energy-efficient inference, Use of AI in VLSI architecture exploration and design-space optimization	**8**	**Apply CO5**

Course Outcomes: After completing the course, the students will be able to	
25VDEP2151.1	Understand the integration of AI techniques in VLSI design for power efficiency.
25VDEP2151.2	Apply hybrid AI models to estimate and reduce power consumption in VLSI circuits.
25VDEP2151.3	Analyze the effectiveness of different AI methodologies in optimizing VLSI system performance.
25VDEP2151.4	Implement AI-driven VLSI designs utilizing contemporary tools and frameworks
25VDEP2151.5	Apply low-power design strategies for integrating hybrid AI models into VLSI systems, focusing on performance, energy efficiency, and hardware constraints.
25VDEP2151.6	Design and simulate VLSI systems incorporating hybrid AI models for enhanced power efficiency.

Reference Books

1. Saini, S., Lata, K., & Sinha, G. R. (Eds.). (2022). VLSI and hardware implementations using modern machine learning methods. CRC Press.
2. Raj, B., Tripathi, S. L., Chaudhary, T., Rao, K. S., & Singh, M. (2024). Integrated devices for artificial intelligence and VLSI. Wiley-Scrivener.
3. Iterative International Publishers. (2024). Advanced VLSI architectures: From concept to silicon. Iterative International Publishers.
4. Janghel, S. R., & Sharma, S. C. (2020). *Hybrid intelligent systems: Analysis and design*. LAP Lambert Academic Publishing.
5. Rabaey, J. M., Chandrakasan, A., & Nikolić, B. (2003). *Digital integrated circuits: A design perspective* (2nd ed.). Pearson Education.

Marks Distribution for Assessment:

<table>
<tr><th rowspan="2">PCC</th><th rowspan="2">CIA</th><th rowspan="2">SEA</th><th colspan="3">CIA (50)</th><th rowspan="2">SEA
Conduction: 100 M
Reduced to: 50 M</th></tr>
<tr><th></th><th>I</th><th>II</th></tr>
<tr><td rowspan="4">Conduction</td><td rowspan="4">50</td><td rowspan="4">50</td><td rowspan="2">Written Test</td><td>50</td><td>50</td><td rowspan="3">Five questions with each of 20 marks (with internal choice). Student should answer one full question from each module</td></tr>
<tr><td colspan="2">Average of two tests – 25 Marks</td></tr>
<tr><td>Assignment</td><td colspan="2">15</td></tr>
<tr><td>AAT</td><td colspan="2">10</td></tr>
<tr><td colspan="4">Total – 50 marks</td><td>Total – 50 marks</td></tr>
</table>

B.N.M. Institute of Technology

An Autonomous Institution under VTU

Dept. of Electronics and Communication Engineering

M. Tech (VLSI Design and Embedded Systems)

Semester: I

Course Name : Memory design for Low Power VLSI System **Code: 25VDEP2152**

L: T:P: J	**3:0:2:0**	**CIA Marks:** 50
Credits:	**4**	**SEA Marks:** 50
Hours	**50**	**SEA Duration: 0**3 Hours

Pre-Requisites: Digital Logic Design, Basic VLSI Design / CMOS Design, Semiconductor Devices, Computer Architecture (Basics)

Course Learning Objectives: The students will be able to

1	To enable students to understand low power design concepts in VLSI and analyze memory architectures and specialized memory cells for power-efficient systems.
2	To impart knowledge on memory constituent subcircuits and develop an understanding of reliability, noise, fault tolerance, and radiation effects in memory design.
3	To provide insights into non-volatile memory technologies, their operational principles, and evaluate performance metrics such as speed, durability, and efficiency.
4	To study low power memory access, leakage reduction techniques, and memory compiler-based optimization for efficient memory design.
5	To understand RAM fault models, test algorithms, and built-in self-test (BIST) techniques for reliable memory testing.

Module -1: Introduction to Low Power Design and Memory Cell

	No. of Hrs	**Bloom's Cognitive Levels**
Introduction: Need for low power VLSI chips, charging and discharging capacitance, short circuit current in CMOS leakage current, static current, basic principles of low power design, low power figure of merits. **Random Access memories**- Fundamental, DRAMs – 1T,3T, SRAMs – 4T,6T, Sequential Access Memories, Content Addressable Memories. Memory Cells- Tunnel Diode Based Memory Cell, Multi Memory Cell, Derivative Memory Cell. Refer Text Book 1.	8	Apply CO1

Module -2: Memory Constituent Subcircuits and Reliability & Yield Improvement

Memory Constituent Subcircuits- Array Wiring, Reference Circuits, Decoders, Output Buffers, Clock Circuits. Reliability and Redundancy, Noise in Memory Circuits, Yield and Redundancy, Fault Tolerance in Memory Designs, Fault Repairs. Radiation Effects. Refer Text Book 1.	8	Apply CO2

Module–3: Fundamentals of Non-Volatile Memories and Performance Figure

Non-Volatile Storage Element: Cell Operation Mode, Non-Volatile Cell: Electron and Non electron based, Flash Memory Array, Memory Building Blocks. Performance Figures: Memory performance Definition, Performance parameters of Flash Memories, Performance and Durability. Refer Text Book 2.	8	Analyze CO3

Module–4: Memory Architecture Optimization Techniques

Low Power Memory Access Techniques- Bit-line and word-line switching minimization, Dual-VDD and dual-VTH memory cells, Pulse-mode techniques for reduced dynamic power, Sense amplifier optimization for power saving. **Banking and Partitioning of Memory Arrays-** Splitting large memories into banks to reduce capacitance and power. Techniques: Access time vs. power trade-off in multi-bank memory, Adaptive bank selection, Row/column multiplexing strategies. **Memory Leakage Reduction Techniques-** Standby leakage reduction (sleep transistors, retention mode), State-preserving power gating in SRAM arrays, Data-aware write suppression, Refresh optimization in DRAM. **Memory Compiler Optimization-** Use of memory	8	Analyze CO4

compilers to generate custom memory macros, Power/performance tuning using compiler options, Constraints-driven generation: area, access time, power. Refer Text Book 3.		
Module–5: Testing and Reliability in Low Power Memory		
RAM Fault design, Test algorithms for RAMs, Detection of Pattern sensitive Faults, BIST Architecture, BIST Techniques for RAM Chips, Test Generation and BIST for Embedded RAMs. Refer Text Book 4.	8	Evaluate CO5

Course Outcomes: After completing the course, the students will be able to	
25VDEP2152.1	Apply low power design principles to analyze power dissipation in CMOS circuits and memory cells, and evaluate different memory architectures for their suitability in low power applications.
25VDEP2152.2	Apply fault tolerance and redundancy techniques while analyzing noise, fault models, and radiation effects to enhance memory reliability and yield.
25VDEP2152.3	Apply knowledge of non-volatile memory cell operation to design flash memory arrays and evaluate their performance parameters including speed, endurance, and durability.
25VDEP2152.4	Apply architectural and circuit-level techniques to optimize memory power consumption, analyze trade-offs in memory banking and partitioning, and evaluate memory compiler options for power and performance optimization.
25VDEP2152.5	Apply RAM fault models and test algorithms to design BIST architectures and evaluate their test coverage and fault detection efficiency for embedded RAMs.

Reference Books

1. CMOS Memory Circuits, Tegze P. Haraszti, Kluwer Academic, E-Book Publisher: Springer, ISBN-13: 978-1475784107. Publication Date: March 21, 2013
2. Flash Memories, Detlev Richter, Spinger, ISBN 978-94-007-6081-3, 2014
3. Advanced Memory Optimization Techniques for Low-Power Embedded Systems, Manish Verma, Peter Marwedel, Publisher: Springer. ISBN-13 978-1-4020-5896-7, April 2013
4. Digital Circuit Testing and Testability by Parag K Lala, Academic Press

Marks Distribution for Assessment:

PCC	CIA	SEA	CIA (50)			SEA Conduction: 100 M Reduced to: 50 M
				I	II	
Conduction	50	50	Written Test	50	50	Five questions with each of 20 marks (with internal choice). Student should answer one full question from each module
				Average of two tests – 25 Marks		
			Assignment	15		
			AAT	10		
			Total – 50 marks			**Total – 50 marks**

B.N.M. Institute of Technology

An Autonomous Institution under VTU

Dept. of Electronics and Communication Engineering

M. Tech (VLSI Design and Embedded Systems)

Semester: I

Course Name: Power semiconductor devices and Technology **Course Code: 25VDEP2153**

L: T: P: J	**3: 0: 0 :0**	**CIE Marks: 50**
Credits:	**3**	**SEE Marks: 50**
Hours/Week	**3**	**SEE Duration: 03 Hours**

Pre-Requisites: Embedded Systems and Sensors

Course Learning Objectives: The students will be able to

1	To provide a basic understanding of power device characteristics and their role in power electronics.
2	To build core understanding of semiconductor behavior and carrier dynamics for electronic device principles.
3	To understand the breakdown mechanisms and conduction limits in semiconductor devices for effective analysis and material selection in power applications.
4	To understand the structural features and key electrical behaviors of advanced rectifiers and transistor devices used in power electronics.
5	To understand the structure, operation, and performance factors of advanced SiC-based power devices for high-efficiency power applications.

Module-1: Introduction	**No. of Hours**	**Blooms cognitive Levels**
Ideal And Typical Power Device Characteristics, Unipolar Power Rectifiers, Bipolar Power Rectifiers, Unipolar Power Transistors, Bipolar Power Devices, MOS- Bipolar Power Devices	**8**	**Understand CO1**
Module-2: Material Properties		
Fundamental properties, energy band gap, intrinsic carrier concentration, junction built-in potential, zero bias depletion width, bulk electron mobility, bulk hole mobility, channel electron mobility, electron velocity field curve, hole velocity field curve	**8**	**Understand CO2**
Module-3: Breakdown Voltage		
Breakdown voltage: parallel plane breakdown, punch through breakdown, open base transistor breakdown, ideal specific on-resistance for one dimensional case, for silicon carbide, for gallium nitride	**8**	**Understand CO3**
Module-4: Schottky Rectifiers and P-i-N Rectifiers		
Schottky Rectifiers structure: Forward Conduction, Reverse Blocking, Shielded Schottyky Rectifiers- Junction Barrier, P.i.N Rectifiers, structure, reverse blocking, reverse recovery, JFET Structure, SiC Planar power MOSFET structure.	**8**	**Understand CO4**
Module-5: Silicon Carbide Power devices		

SiC BJT:structure and operation, breakdown voltage, current gain, SiC Gate turn off thyristors: structure and operation, forward blocking capability, switching characteristics, SiC IGBTs:n channel Asymmetric Structure, optimized n channel asymmetric structure, p-channel asymmetric structure.	**8**	**Understand CO5**

Course Outcomes: After completing the course, the students will be able to	
25VDEP2153.1	Students will be able to describe key power device characteristics and their applications in power electronics systems.
25VDEP2153.2	Students will be able to explain semiconductor behavior and carrier dynamics essential to electronic device operation.
25VDEP2153.3	Students will be able to analyze breakdown mechanisms and conduction limits in semiconductor devices to guide material and device selection for power applications.
25VDEP2153.4	Students will be able to explain the structural design and electrical characteristics of advanced rectifiers and transistor devices in power electronics.
25VDEP2153.5	Students will be able to analyze the structure and operation of advanced SiC power devices and evaluate their performance characteristics for efficient power system design.

Reference Books

1. B. J. Baliga, *Gallium Nitride and Silicon Carbide Power Devices*, World Scientific, 2017.
2. HongyuYu, TianliDuan, *Gallium Nitride Power Devices*, Pan Stanford, 2017
3. Research articles and technical reports in the area of Power semiconductor device experimentation, modeling and Fabrication.
4. B. Jayant Baliga, Fundamentals of Power Semiconductor Devices, Springer, 2008
5. B. J. Baliga., *Silicon Carbide Power Devices*, World Scientific, 2006.
6. Baliga, B. Jayant, *Power Semiconductor Devices*, PWS Publishing Co., Boston, 1996.

B.N.M. Institute of Technology

An Autonomous Institution under VTU

Dept. of Electronics and Communication Engineering

M. Tech (VLSI Design and Embedded Systems)

Semester: I

Course Name: Computer Aided Design of VLSI Circuits **Code:25VDEP2154**

L: T: P: J	**3 : 0 : 0: 0**	**CIA Marks:** 50
Credits:	**3**	**SEA Marks:** 50
Hours/Week (Total)	**40**	**SEA Duration:** 03 Hours

Pre-Requisites: Understanding of digital electronics basic concepts of VLSI architecture, design flow, CMOS technology, and layout design, knowledge of data structures such as trees, graphs, stacks, and queues used in optimization and physical design algorithms, Basic proficiency in programming languages such as C/C++ or Python, exposure to any EDA/CAD tools like Cadence, Synopsys, or Mentor Graphics

Course Learning Objectives: The students will be able to

1	Understand the concept of digital systems, how they can be optimized for area, power and cost, why it is advantageous to use physical design tools.
2	Implement the concept of the physical design cycle and develop algorithms (tools) for each design cycle step and optimize the digital system at architectural level.
3	Synthesize a given system starting with problem requirements, identifying and designing the building blocks, and then integrating blocks designed earlier
4	Develop their own platform (tool) for specific application.

Module-1	**No. of Hours**	**Blooms cognitive Levels**
High Level Synthesis: Hardware models - Internal representation - Allocation assignment and scheduling - Simple scheduling algorithm - Assignment problem – High level transformations. **VLSI Simulation:** Gate-level modelling and simulation - Switch-level modelling and simulation - Combinational Logic Synthesis - Binary Decision Diagram.	**8**	**Apply CO1**
Module-2		
Data Structure and Basic Algorithms: Basic Terminology, Graph Search Algorithms Computational Geometry Algorithms. **VLSI partitioning& floor planning**: Problem Formulation, Classification of Partitioning Algorithms, Group migration Algorithms, Simulated Annealing and evolution algorithm, other partitioning algorithms. Problem formulation, classification, Constraint based, Integer programming based, rectangular dualization, simulated evolution floor planning algorithms.	**8**	**Apply CO2**
Module-3		
Placement and Routing: Problem formulation, Classification, Simulation based, Partitioning based Placement Algorithms. **Global Routing:** Problem formulation, Classification, Maze routing Algorithms, Line Probe Algorithms, shortest path based Algorithms, Steiner tree based Algorithms Detailed Routing: Problem formulation, Classification single Layer routing, General river routing, Single row roting.	**8**	**Apply CO3**
Module-4		
Clock and Power Routing: Design considerations for the clocking system, delay calculation for clock trees, Problem formulation, Clock routing Algorithms, H-tree based Algorithms, MMM Algorithms, Geometric matching based Algorithms. **Compaction:** Classification of Compaction Algorithms, One-Dimensional &Two-Dimensional Compaction, Hierarchical Compaction	**8**	**Apply CO4**

Module-5		
Genetic algorithm and its application in VLSI physical design: Terminologies – Simple Genetic algorithms, steady state algorithm – Genetic operators-types of GA-Genetic algorithms vs Conventional algorithms – GA example – GA for VLSI design. Genetic algorithm in portioning, placement and routing.	**8**	**Apply CO5**

Course Outcomes: After completing the course, the students will be able to	
25VDEP2154.1	Analyse each stage of VLSI design flow.
25VDEP2154.2	Apply design knowledge to develop algorithms for VLSI design automation
25VDEP2154.3	Investigate the algorithms for optimizing VLSI design with respect to speed, power and area.
25VDEP2154.4	Design an optimized VLSI cell using various algorithms.
25VDEP2154.5	Utilize genetic algorithms to solve VLSI design problems such as partitioning, placement, and routing, and compare their effectiveness with traditional methods.

Reference Books

1. Pinaki mazumder and Elizabeth M Rudnick, "Genetic algorithms for VLSI design layout and test automation", Pearson Edition, 2011.
2. N.A. Sherwani, "Algorithms for VLSI Physical Design Automation", Kluwar Academic Publishers, 2002, ISBN: 0-7923-8393-1
3. S.H. Gerez, "Algorithms for VLSI Design Automation", John Wiley & Sons, 1998, ISBN: 978-0-471-98489-4

Marks Distribution for Assessment:

<table>
<tr><th>PBL</th><th>CIA</th><th>SEA</th><th colspan="3">CIA (50)</th><th>SEA
Conduction: 100 M
Reduced to: 50 M</th></tr>
<tr><td rowspan="5">Conduction</td><td rowspan="5">50</td><td rowspan="5">50</td><td rowspan="3">Theory</td><td>I IA</td><td>II IA</td><td rowspan="4">Five questions with each of 20 Marks (with internal choice).
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<tr><td>Assignment</td><td colspan="2">15</td></tr>
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</table>

B.N.M. Institute of Technology

An Autonomous Institution under VTU

Dept. of Electronics and Communication Engineering

M. Tech (VLSI Design and Embedded Systems)

Semester: I

Course Name: RESEARCH METHODOLOGY AND IPR **Code: 25VDE216**

L: T :P: J: 0	**3: 0 : 0 : 0**	**CIA Marks:** 50
Credits	**3**	**SEA Marks:** 50
Hours/Week (Total)	**3 (40)**	**SEA Duration:** 03 Hours

Pre-Requisites: Use of internet and online database, clarity on research question/problem and basic of statistics

Course Learning Objectives: The students will be able to

1	To give an overview of the research methodology and explain the technique of defining a research problem
2	To explain the functions of literature review, carry out literature search and develop conceptual frameworks
3	To explain various experimental designs in research and data handling like data sampling and data collection methods
4	To interpret the research findings and prepare a research report
5	To build awareness on the various forms of IPR and manage a project and the related finances independently.

Module-1: Introduction to Research Methodology	**No. of Hours**	**Blooms Cognitive Levels**
Research Methodology: Introduction, Meaning of Research, Objectives of Research, Motivation in Research, Types of Research, Research Approaches, Significance of Research, Research Methods versus Methodology, Research and Scientific Method, Importance of Knowing How Research is Done, Research Process, Criteria of Good Research **Defining the Research Problem**: Research Problem, Selecting the Problem, Necessity of Defining the Problem, Technique Involved in Defining a Problem, An Illustration Problems Encountered by Researchers in India.	**08**	**Apply CO1**
Module-2: Literature Review		
Reviewing the literature: Place of the literature review inresearch, bringing clarity and focus to your research problem, Improving research methodology, Broadening knowledge base in research area, enabling contextual findings, How to review the literature, searching the existing literature, reviewing the selected literature, developing a theoretical framework, Developing a conceptual framework, writing about the literature reviewed. **Research Design**: Meaning of Research Design, Need for Research Design, Features of a Good Design, Important Concepts Relating to Research Design, Different Research Designs, Basic Principles of Experimental Designs, Important ExperimentalDesigns.	**08**	**Apply CO2**
Module-3: Data Sampling and Testing of Hypothesis		

Design of Sampling: Introduction, Sample Design, Sampling andNon-sampling Errors, Sample Survey versus Census Survey, Types of Sampling Designs. **Measurement and Scaling**: Qualitative and Quantitative Data, Classifications of Measurement Scales, Goodness of Measurement Scales, Sources of Error in Measurement Tools, Scaling, Scale Classification Bases, Scaling Technics, Multidimensional Scaling, Deciding the Scale. **Data Collection:** Experimental and Surveys, Collection of Primary Data, Collection of Secondary Data, Selection of Appropriate Method for Data Collection. **Testing of Hypotheses**: Hypothesis, Basic Concepts Concerning Testing of Hypotheses, Testing of Hypothesis, Test Statistics and Critical Region, Critical Value and Decision Rule.	**08**	**Apply CO3**
Module-4: Interpretation and Report Writing		
Interpretation: Meaning of Interpretation, Technique of Interpretation, Precaution in Interpretation. **Report Writing:** Significance of Report Writing, Different Steps in Writing Report, Layout of the Research Report, Types of Reports, Oral Presentation, Mechanics of Writing a Research Report, Precautions for Writing Research Reports.	**08**	**Analyze CO4**
Module-5: Intellectual Property Rights and Project Management		
Intellectual Property Rights: Intellectual Property: The Concept, Intellectual Property System in India, Development of TRIPS Complied, Regime in India, Various patent and deign acts of India. **Project Management:** Definition of project, characteristics of projects, types of projects, project roles. Strategic planning process, strategic objectives, identifying potential projects, feasibility study (environment, society), methods of selecting projects, prioritizing projects, securing and negotiating projects.	**08**	**Apply CO5**

Course Outcomes: After completing the course, the students will be able to	
25VDE216.1	Apply understanding to formulate a clearly defined research problem.
25VDE216.2	Apply the theoretical knowledge of literature survey to carry out literature review for a paper publication
25VDE216.3	Implement appropriate sampling techniques and data collection methods in a research context.
25VDE216.4	Interpret the research findings and create a report
25VDE216.5	Apply principles of Intellectual Property Rights (IPR) and project management in real-world project scenarios.

Reference Books

1. C.R. Kothari, Gaurav Garg, "Research Methodology: Methods and Techniques", New Age International 4th Edition, 2018.
2. Ranjit Kumar, "Research Methodology a step-by-step guide for beginners" (For the topic Reviewing the literature under module 2), SAGE Publications 3rd Edition, 2011.
3. John J Hampton, Financial Management, PHI Publication, 4th edition, 2020Trochim, "Research Methods: the concise knowledge base", Atomic Dog Publishing 2005.
4. Fink A, "Conducting Research Literature Reviews: From the Internet to Paper", Sage Publications 2009.
5. Timothy J Kloppenborg, Project Management, Cengage Learning, 2nd Edition, 2019.

Marks Distribution for Assessment:

PCC	CIA	SEA	CIA (50)			SEA Conduction: 100 M Reduced to: 50 M
				I	II	
Conduction	50	50	Written Test	50	50	Five questions with each of 20 marks (with internal choice). Student should answer one full question from each module
				Average of two tests – 25 Marks		
			Assignment	15		
			AAT	10		
			Total – 50 marks			**Total – 50 marks**