BNM Institute of Technology

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IEEE Circuits and Systems Society (SBC 14831A)

List of Events Organized in 2025

Sl. No	Event Title	Date	No. of Participants
1	Awareness Workshop on Semiconductor Technologies	19th December 2025	53
2	Circuit Theatre – IEEE Week 2025	16th October, 2025	60
3	NXP Campus Connect Webinar on "SRAM and ROM IP Architecture and Design	02nd September, 2025	50
4	Internship on Design, Modeling, and Simulation of Digital Circuits using Verilog	21st July, 2025 to 09th August 2025	64
5	Industrial Visit to BMRCL	12th July 2025	135
6	Industrial Visit to DSedify	4th July, 2025	50
7	Technical Talk on VLSI Industry Prospects: Core Opportunities for ECE Graduates	27th June 2025	100
8	Masterclass on Higher Education (Abroad Studies)	26th June 2025	42
9	Internship on Design Verification using System Verilog	02nd June 2025 to 20th June 2025	64

10	Avinya 2025 – Project Exhibiton	12th May 2025	120

IEEE CAS BNMIT Office Bearers

Sl. No	Name	Position Held
1	Debarati Mukherjee	Chair
2	Manish L, Harshini H L	Vice-Chair
3	Shreyas S, Manjushree S	Secretary
4	Dhruv M N	Treasurer
5	Akanksha Sharma, Amogh M S	Webmaster

Faculty Advisor : Dr. Yasha Jyothi M Shirur

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Title of the Event: "Awareness Workshop on Semiconductor Technologies"

Date: 19th December, 2025 Time: 11:30 AM to 12:30 PM

Venue: N Block, N-401, Seminar Hall, BNMIT Participants: 53

Organized by:
IEEE Circuits and Systems Society – BNMIT Student Branch Chapter and IEEE BNMIT Student Branch Chapter
B.N.M. Institute of Technology (Autonomous), Bengaluru

Overview :

The Department of Electronics and Communication Engineering, BNMIT organized a Awareness Workshop on Semiconductor Technologies in collaboration with the IEEE Circuits and Systems Society Student Branch.

Event Proceedings :

1. The Awareness Workshop on Semiconductor Technologies was organized by the Department of Electronics and Communication Engineering, BNMIT, with the aim of creating awareness among students about semiconductor technology and its growing importance in modern electronics and communication systems. The workshop focused on helping students understand the practical relevance of concepts that they study in their academic curriculum.
2. Experts from the Centre for Nano Science and Engineering (CeNSE), IISc conducted the session and shared their valuable knowledge and experience in the field of semiconductor technologies. They explained the fundamentals of semiconductors, fabrication processes, and recent advancements taking place in the semiconductor industry.
3. The speakers discussed how semiconductor devices play a crucial role in the functioning of various electronic systems such as smartphones, computers, communication equipment, and embedded systems. The session helped students understand the wide range of applications of semiconductor technologies in everyday life.
4. The workshop also highlighted the rapid growth of the semiconductor industry and the increasing demand for skilled professionals in this field. Students were encouraged to explore opportunities in semiconductor research, higher studies, and industry-related careers.
5. The session included an interactive discussion where students actively participated and clarified their doubts related to semiconductor technologies, research facilities, and the skills required to build a career in this domain.
6. Overall, the workshop was highly informative and beneficial for the students as it successfully connected theoretical learning with real-world applications. The Department of Electronics and Communication Engineering, BNMIT expressed sincere gratitude to the CeNSE, IISc team for their valuable contribution and support in making the workshop a success.

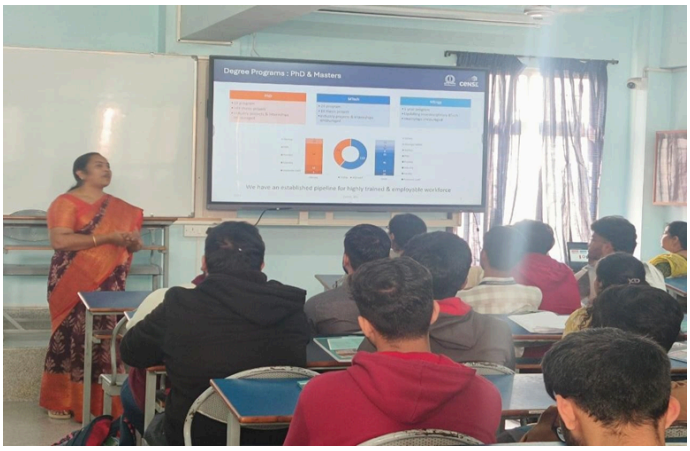
Objective :

- The primary objectives of the workshop were to:
- Create awareness about semiconductor technologies and fabrication processes
- Introduce students to CeNSE facilities and cleanroom infrastructure at IISc
- Highlight industry–academia collaboration in semiconductor research
- Provide information on higher education opportunities (M.Tech, MS, PhD) at IISc
- Motivate students to pursue careers in VLSI, nanoelectronics, and semiconductor industries

Conclusion :

The Awareness Workshop on Semiconductor Technologies was highly informative and impactful. It successfully bridged the gap between classroom learning and real-world semiconductor applications. The Department of Electronics and Communication Engineering, BNMIT, expresses sincere gratitude to the CeNSE, IISc team for their valuable contribution and looks forward to continued collaboration in the future.

Event Images :



BNM Institute of Technology

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Title of the Event: "Circuit Theatre – Bringing Electronics to Life"

Date: 16th October, 2025 Time: 11:00 AM to 3:40 PM

Venue: S-006, BNMIT Participants:

Organized by:
IEEE BNMIT Student Branch Chapter and
IEEE Circuits and Systems Society – BNMIT Student Branch Chapter and
B.N.M. Institute of Technology (Autonomous), Bengaluru

Overview :

The Department of Electronics and Communication Engineering, in association with the IEEE Circuits and Systems (CAS) Society, BNMIT, organized an innovative and interactive event titled *"Circuit Theatre"* as part of IEEE Week 2025.The event aimed to combine creativity with technical knowledge by allowing students to enact and dramatize electronic circuits and systems. Each team represented components such as resistors, capacitors, diodes, and transistors, bringing them to life through theatrical performances. This initiative provided students with an engaging platform to understand circuit behavior while encouraging teamwork and public speaking.

Event Proceedings :

1. The event "Circuit Theatre" was organized by the Department of Electronics and Communication Engineering in association with the IEEE Circuits and Systems (CAS) Society, BNMIT as part of IEEE Week 2025. The event aimed to create an innovative learning environment where students could combine creativity with technical knowledge by dramatizing electronic circuits and systems.
2. The event began with a warm welcome by the organizing committee, followed by a brief introduction about the concept of the event and its objectives. The participants were informed about the rules, judging criteria, and the overall flow of the program before the performances began.
3. A total of 12 teams participated in the event, mainly consisting of first-year and second-year ECE students. Each team had 3–5 members who collaborated to design creative skits based on different electronic circuits and systems, demonstrating both their technical understanding and creativity.
4. During the performances, students enacted the roles of various electronic components such as resistors, capacitors, diodes, and transistors. Through dialogues, storytelling, and dramatization, they explained how these components function within different circuits such as amplifiers, flip-flops, filters, communication systems, and logic gates.
5. Participants creatively used props, charts, and sound effects to make their performances more engaging and entertaining. The event successfully blended technical explanations with humor and storytelling, which made the learning process enjoyable for both participants and the audience.

6. The performances displayed a high level of creativity, teamwork, and conceptual clarity. One team presenting the theme of a Low Pass Filter secured the first place for their strong technical explanation and engaging performance, while the second place was shared by two teams who demonstrated excellent coordination and innovative presentations.
7. The event was evaluated by Mr. Kiran K. N, Assistant Professor from the Department of ECE, BNMIT, who judged the teams based on technical understanding, creativity, presentation skills, and teamwork demonstrated during the performances.
8. The award distribution took place in the presence of Dr. Yasha Jyothi M. Shirur, Head of the Department of ECE, BNMIT, and Dr. Priyadarshini K. Desai, Assistant Professor, Department of ECE, BNMIT, who appreciated the efforts and enthusiasm shown by the students.
9. The event provided students with an opportunity to improve their conceptual understanding of circuits while also developing important skills such as communication, confidence, teamwork, and creative thinking.

Objective :

- To promote enthusiasm and creativity among students in the field of electronics.
- To enhance conceptual understanding of circuits and systems through performance-based learning.
- To encourage teamwork, communication, and innovation in presenting technical concepts.
- To create a fun, interactive learning atmosphere as part of IEEE Week celebrations.

Conclusion :

The event *"Circuit Theatre"* was a grand success, achieving its goal of making electronics learning engaging and memorable. The fusion of drama and circuits captured the interest of young engineers and highlighted the creative spirit of BNMIT's ECE community.The event concluded with a snack distribution session, where participants and faculty members interacted informally, sharing feedback and appreciation for the performances. The IEEE CAS Society, BNMIT, looks forward to conducting more such events that blend technical learning with creativity, ensuring active student participation and experiential growth.

Event Images :


GPS Map Camera
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Whc9+p7m, Banashankari Stage Ii, Banashankari, Bengaluru,
Karnataka 560070, India
Lat 12.921876° Long 77.568032°
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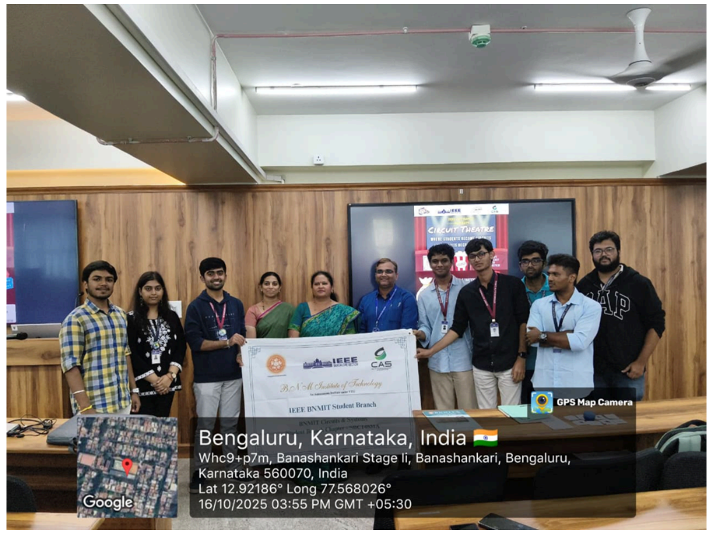
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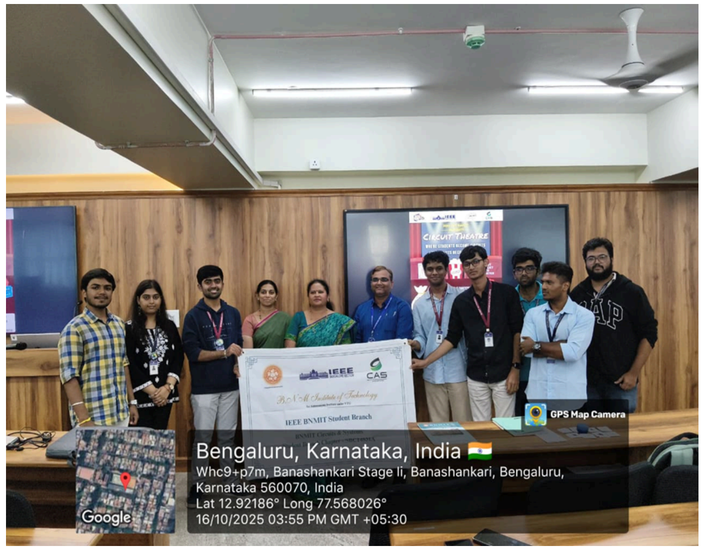
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B.N.M Institute of Technology

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Department of Electronics & Communication Engineering

REPORT

Title	NXP Campus Connect Webinar on *"SRAM and ROM IP Architecture and Design"*
Number of Students participated	50
Semester/Section	ECE Students
Date & Time	02nd September 2025 5.00 TO 6.00 PM
Staff Coordinators	• Dr. Vrunda Kusanur, Associate Professor, ECE • Dr. Smitha Gayathri D, Associate Professor, ECE

SESSION IS HOSTED BY

NXP Campus Connect

Webinar Topic: SRAM and ROM IP Architecture and Design

LIVE SESSION

SRAM and ROM IPs are critical in modern SoCs, occupying significant chip area and influencing system performance, power, and functionality. This session introduces basic building blocks, operations, and functionality, and highlights how different architectural choices impact the overall PPA (Power, Performance, Area) of memory Ips.

SPEAKERS

Rajat Kohli
Sr. Principal Engineer / Design Manager e-Memories
NXP Semiconductors

To attend the session In-Person

Tuesday

2nd September

5:00 – 6:00 pm IST

Concept Hall, S Block, S-106

Join Virtually

Write to us at: nxpcampus.connect_1@nxp.com

Connect with us at:
Website: www.nxp.com
LinkedIn: https://www.linkedin.com/in/nxpcampusconnect/
YouTube: https://www.youtube.com/@NXPIndiaCommunication

Introduction

The Department of Electronics and Communication Engineering, BNMIT, in collaboration with **NXP Campus Connect**, organized a webinar on *"SRAM and ROM IP Architecture and Design."* The session emphasized the critical role of memory IPs in SoC design, covering fundamentals, design trade-offs, and real-world applications.

The event began with a warm welcome by Mr. Manish L (5th Sem ECE, Treasurer – BNMIT IEEE CASS Chapter), followed by the felicitation of dignitaries. Dr. S. Y. Kulkarni (Additional Director & Principal, BNMIT) addressed the gathering and shared encouraging words.

Following this, Dr. Yasha Jyothi M. Shirur (HoD, Department of ECE) provided an overview of the institution, highlighting BNMIT's focus on research-driven learning, industry collaborations, and student-centered initiatives that nurture innovation and technical excellence.

Ms. Aadya then introduced the Chief Guest, highlighting Mr. Rajat Kohli's distinguished career spanning over two decades, his contributions at ARM, STMicroelectronics, and NXP, as well as his patents and recognitions in semiconductor memory architectures.

Technical Session:

Mr. Rajat Kohli delivered an engaging talk on **SRAM and ROM IPs**, covering:

- Fundamentals of memory IP design.
- Architecture and building blocks of SRAM and ROM.
- The impact of design choices on **Power, Performance, and Area (PPA)**.
- Real-world semiconductor challenges and innovative solutions.

The session was highly interactive and included a Q&A segment where students clarified their technical queries directly with the speaker.

Participation:

The event witnessed enthusiastic participation from **over 50 students**, along with faculty members and coordinators. The hybrid format enabled both in-person and virtual attendees to benefit from the session.

Key Outcomes:

- Students gained practical industry insights on memory IP design.
- The session bridged the gap between academic learning and real-world applications.
- Encouraged students to explore semiconductor research, VLSI, and SoC design as career opportunities.

Acknowledgements:

We express our sincere gratitude to Mr. Rajat Kohli Sir for his valuable session, and to our dignitaries — Dr. S. Y. Kulkarni Sir, Dr. Yasha Jyothi M. Shirur Madam, and Prof. Satish Kumar Sir — for their guidance and presence.

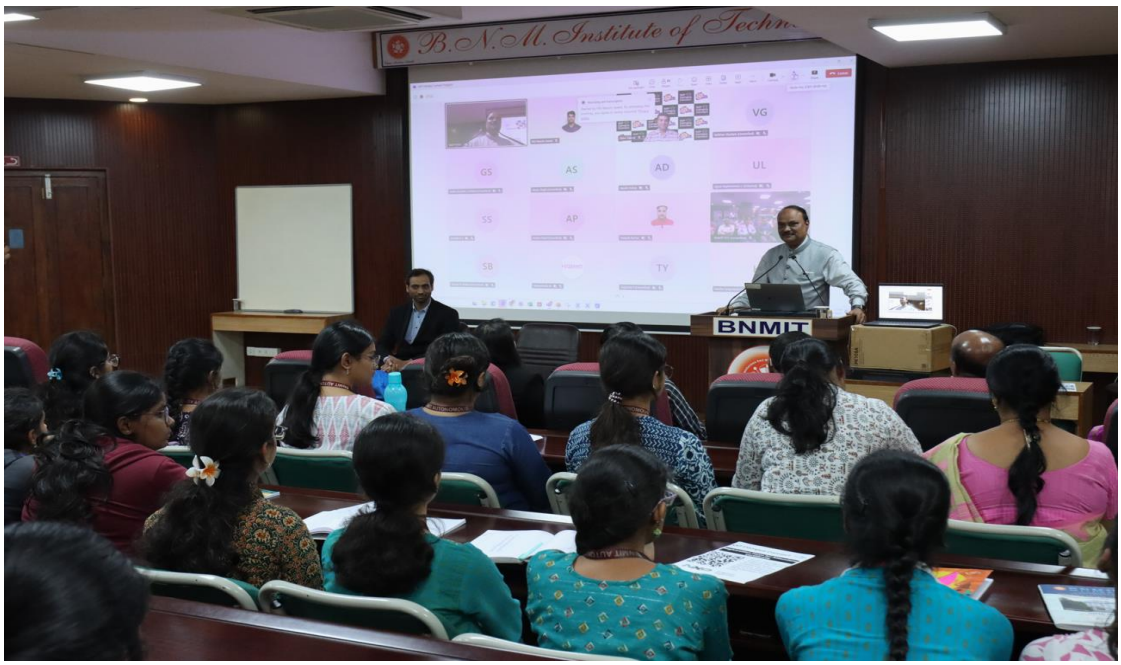
We also gratefully acknowledge the constant support of our institution leaders — Shri. Narayan Rao Maanay Sir, Prof. T. J. Ramamurthy Sir, Prof. Eeshwar N. Maanay Sir, and Dr. Krishnamurthy G. N Sir — whose encouragement enables such initiatives.

Special thanks to the event coordinators Dr. Vrunda Kusanur and Dr. Smitha Gayathri D for successfully organizing the event.

Conclusion:

The webinar was a grand success, leaving students motivated and better informed about advanced memory IP architecture and design. The insights shared by Mr. Rajat Kohli served as an inspiration to budding engineers to pursue excellence in the field of semiconductor technology and VLSI design.

"Group photograph of dignitaries, faculty, and students during the NXP Campus Connect Webinar on *'SRAM and ROM IP Architecture and Design'* organized by IEEE BNMIT CASS Chapter. The event witnessed active participation and insightful interactions, making it a memorable learning experience."



"Dr. S. Y. Kulkarni, Additional Director & Principal of BNMIT, addressing the gathering during the NXP Campus Connect Webinar. The session witnessed enthusiastic participation, blending in-person and virtual interactions."

"Mr. Rajat Kohli, Senior Principal Engineer at NXP Semiconductors, delivering a technical session on SRAM and ROM IP Architecture and Design, engaging students with in-depth insights into memory operations."

"Dignitaries and faculty members of BNMIT with Mr. Rajat Kohli, Senior Principal Engineer at NXP Semiconductors, during the NXP Campus Connect Webinar."

Coordinator HOD-ECE

B.N.M. Institute of Technology

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NXP Campus Connect Program – 02.09.2025

Venue:A215 **Time: 5.00pm**

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100.	24ece054@bnmit.in	Sannidhi S Rao	1BG24EC082	ECE	3rd sem	8123359875	
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102	24ece047@bnmit.in	Shreya KC	1BG24EC088	ECE	3rd sem	9611365197	
103	24ece063@bnmit.in	Ramya C.S	1BG24EC071	ECE	3rd sem	9980270159	Ramya
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105	24ece095@bnmit.in	Anshika M.G	1BG24EC017	ECE	3rd sem	8660174543	

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					IIIrd Sem	9036560818
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116)	Tejas N. 24ece089@bnmit.in	Tejas 'N'		ECE	III sem	9108117927
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118)	24ece065@bnmit.in	RITHVIK SHRIRAM	1BG24EC074	ECE	III Sem	9945082737
119)	24ece096@bnmit.in	Varun.S	1BG24EC112	ECE	III sem	9606059350
120)	24ECE083@bnmit.in	Rajath.R.K	1BG24EC065	ECE	III Sem	7483636715
121)	24ece029@bnmit.in	Samarth.R.B	1BG24EC078	ECE	III Sem	8073853734
122)	24ece105@bnmit.in	Ramesh.N	1BG24EC070	ECE	III sem	9663549238
123)	24ece104@bnmit.in	Rishi.R	1BG24EC073	ECE	III sem	9845637033
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127]	24ece092@bnmit.in	chiranthan	1BG24EC023	ECE	III sem	6366212509	chiranthan
128]	24ece022@bnmit.in	chethan kumar.y	1BG24EC022	ECE	III rd sem	9071553376	Chy
129]	24ece004@bnmit.in	DHRUV. M.N	1BG24EC025	ECE	III rd sem	8123074230	Dhruv. M.N
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B.N.M. Institute of Technology

Autonomous Institution under VTU

Department of Electronics and Communication Engineering

INTERNSHIP PROGRAM REPORT

Topic: Design, Modeling, and Simulation of Digital Circuits using Verilog
Tool: Xilinx ISE
Duration: 21-07-2025 to 09-08-2025
Venue: N505 and N506

Organised by:

Department of Electronics and Communication Engineering

In Association with

IEEE CAS, IEEE NANO TECHNOLOGY & IEEE ROBOTICS AND AUTOMATION

Introduction

The Department of Electronics and Communication Engineering, B.N.M. Institute of Technology, organised an internal internship program on "Design, Modeling, and Simulation of Digital Circuits using Verilog" for the 3rd semester ECE students. The program was conducted in three batches (Group A, Group B, and Group C) between 21st July 2025 and 9th August 2025. The internship aimed to provide students with hands-on experience in digital circuit design, simulation, and verification using the Xilinx ISE tool.

Objectives

- To introduce students to Verilog HDL for digital system design.
- To familiarize students with simulation and synthesis tools.
- To demonstrate combinational and sequential circuit design techniques.
- To provide practical exposure to FSM design and verification.
- To encourage students to apply theoretical concepts to practical implementations.

Participants Profile

The internship was attended by 3rd semester students of the ECE department. Students were divided into three groups.

Group A: 21-07-2025 to 25-07-2025

Group B: 28-07-2025 to 01-08-2025

Group C: 04-08-2025 to 09-08-2025

Program Structure

The program was structured into 5 days per batch, with each day having multiple sessions covering different topics in Verilog HDL design and simulation.

Day-wise Summary of Internship

Day 1: Students were introduced to Xilinx ISE, creating projects, and simulating basic gates and adders. Behavioral modeling was explained with examples.

Day 2: Students implemented ripple carry adders and array multipliers using structural and dataflow modeling. Use of operators in Verilog was demonstrated.

Day 3: Multiplexers, encoders, and parity checkers were designed using conditional and case statements.

Day 4: Sequential circuits such as flip-flops were implemented. Blocking vs. non-blocking assignments were demonstrated. Gate-level primitives were introduced.

Day 5: FSMs were designed and simulated. Students implemented sequence detectors and counters. Assessment was conducted through coding tasks and quizzes.

Faculty Involvement

The sessions were delivered by the resource person:

Dr. Subodh Kumar Panda, Professor, ECE Department

Dr. Rekha P, Professor, ECE Department

Dr. Rashmi S B, Associate Professor, ECE Department

Dr. Smitha Gayathri D, Associate Professor, ECE Department

Faculty members rotated across batches to handle specific sessions according to their expertise.

Tools and Facilities Used

- Software: Xilinx ISE Design Suite

- Language: Verilog HDL

- Laboratory: N505 and N506 (ECE Department Digital Design Labs)

Outcomes

By the end of the session, students will be able to:

- Demonstrate proficiency in Verilog HDL coding and simulation techniques.
- Design and verify both combinational and sequential digital circuits.
- Understand and apply different modeling styles in Verilog (structural, dataflow, behavioral).
- Design, implement, and synthesize Finite State Machines (FSMs) using Verilog.

Assessment

At the end of each batch, an assessment was conducted to evaluate the learning outcomes. The assessment consisted of two components:

- **Quiz:** Tested theoretical understanding of Verilog HDL concepts and digital design principles.
- **Practical Programming Task:** Students were given a problem statement and asked to write and execute Verilog code, followed by simulation and verification in Xilinx ISE.

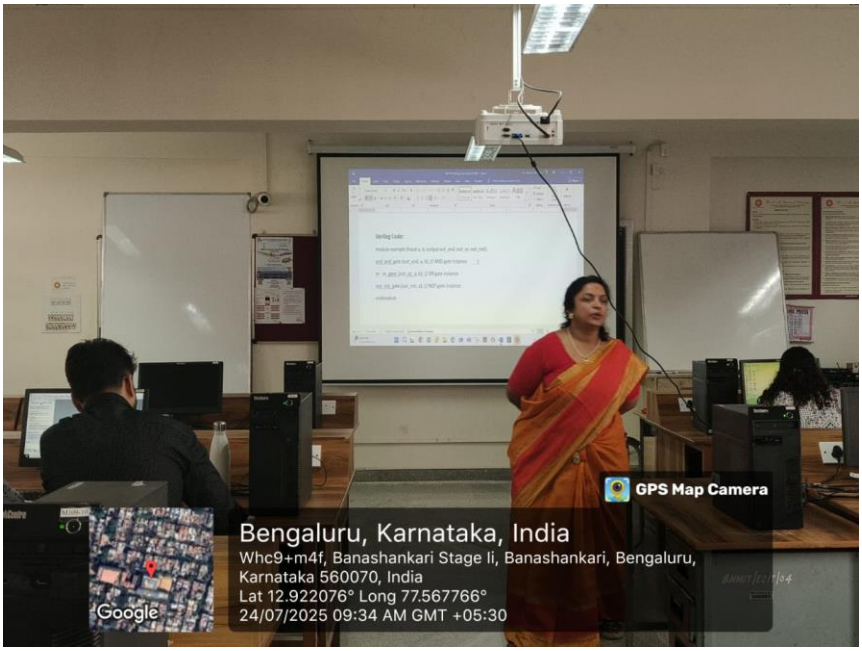
Students were evaluated based on code correctness, logical design, simulation accuracy, and clarity of implementation.

Photo Evidence

Dr. Subodh Kumar Panda, Professor, Department of ECE, delivered an insightful session on Verilog Fundamentals, focusing on various modeling styles—structural, dataflow, and behavioral. The session also covered Verilog syntax, simulation practices, and the design of combinational and sequential circuits, helping students gain a solid foundation in Hardware Description Language (HDL) and digital design principles.

Dr. Rekha P, Associate Professor, Department of ECE, conducted an engaging session on Verilog Operators, Ripple Carry Adder (RCA) using structural modeling, and the implementation of a 2-

bit × 2-bit Array Multiplier using dataflow modeling. The session provided students with hands-on understanding of operator usage in Verilog and practical design examples to strengthen their HDL coding and simulation skills.



Dr. Rashmi S B, Associate Professor, Department of ECE, delivered a detailed session on Finite State Machines (FSMs), focusing on the design and implementation of sequence detectors and counters using Verilog. The session helped students understand state-based design approaches and their practical applications in digital systems through HDL coding and simulation.

Dr. Smitha Gayathri D, Assistant Professor, Department of ECE, conducted an interactive session on Multiplexer, Parity Encoder, and the use of conditional and loop

statements in Verilog. The session emphasized both conceptual understanding and practical implementation, enabling students to write efficient Verilog code for various digital components and control structures.

Group Photo taken during the IEEE student branch event held at BNMIT, featuring student members and faculty coordinators from various IEEE Societies including Robotics & Automation, Nanotechnology Council, and Circuits & Systems. The event was marked by enthusiastic participation and active involvement from both students and faculty, highlighting the collaborative spirit and commitment to technical excellence.

Conclusion

The internship program successfully achieved its objectives by providing students with a solid foundation in digital design using Verilog HDL. The structured schedule, dedicated faculty guidance, and hands-on practice sessions ensured that the learning outcomes were met. The feedback from students indicated a high level of satisfaction and a strong interest in applying these skills to future projects.

Acknowledgment

We thank the Management, Principal, and Head of the Department for their support in organising this program. Special thanks to all faculty members and lab staff for their efforts in conducting the sessions smoothly.

B.N.M Institute of Technology

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Department of Electronics & Communication Engineering

REPORT

Title	**Industrial Visit to BMRCL**
Number of Students participated	**42**
Semester/Section	**5th semester ECE Students**
Date & Time	**12th July 2025 7:30 AM**
Staff Coordinators	• **Dr. Smitha Gayathri D, Associate Professor, ECE** • **Dr. Ashvini Savanth, Associate Professor, ECE**
Organized Under	**IEEE CASS**

1. Introduction

An industrial visit was organized by the **Department of Electronics and Communication Engineering, BNM Institute of Technology**, for the 5th semester students to **Bangalore Metro Rail Corporation Limited (BMRCL), Byappanahalli** on **12th July 2025**. The visit aimed to provide students with practical insights into metro rail operations, infrastructure, communication systems, and control mechanisms used in large-scale public transport systems.

2. About BMRCL

Bangalore Metro Rail Corporation Limited (BMRCL), a joint venture between the Government of India and the Government of Karnataka, is responsible for implementing and operating **Namma Metro** — a rapid transit system serving the city of Bengaluru. The **Byappanahalli depot** is a central hub for metro train maintenance, operation control, and power distribution systems.

This visit provided a behind-the-scenes understanding of how a metropolitan rail transport system is managed, monitored, and maintained to ensure efficiency and safety.

3. Key Highlights of the Visit

- **Briefing Session:** Students were introduced to the operational framework of BMRCL, including project implementation phases, challenges in urban rail systems, and safety protocols.
- **Visit to Operation Control Centre (OCC):**
  Students observed how the metro's **real-time operations** are monitored, including train movement tracking, signal control, and power supply management.

- **Communication and Signaling Systems:**
  Experts explained the **Automatic Train Control (ATC)**, **Signaling**, and **SCADA** (Supervisory Control and Data Acquisition) systems, which play a crucial role in train scheduling and passenger safety.
- **Train Maintenance Facility:**
  Students toured the depot's workshop and learned about **preventive and corrective maintenance** procedures for metro coaches.
- **Energy and Power Systems:**
  An overview of the **third rail electrification system**, energy optimization techniques, and backup systems was provided by technical staff.

4. Student Learning Outcomes

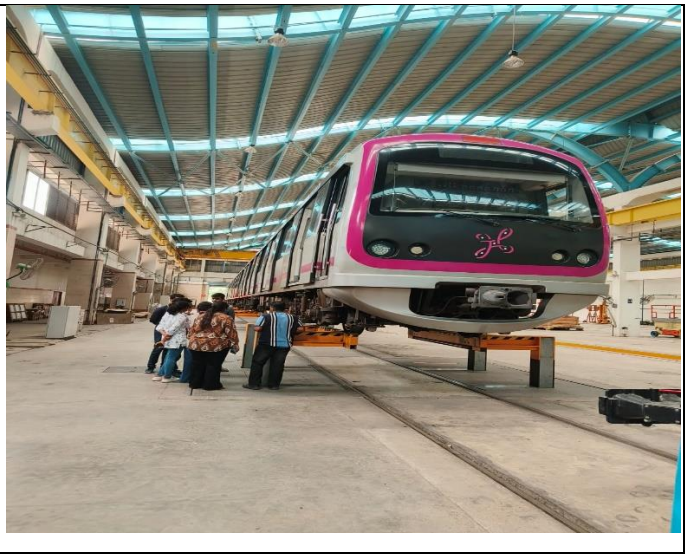
Through this visit, students:

- Gained exposure to **real-world applications of electronics and communication** in the field of transportation and public infrastructure.
- Understood the **integration of embedded systems, communication protocols, and automation** in a metro system.
- Learned about **project planning, execution, and systems engineering** in a large-scale urban mobility solution.
- Enhanced awareness about **career opportunities** in transportation technology and infrastructure planning.

5. Conclusion

The industrial visit to **BMRCL, Byappanahalli** was a highly enriching and informative experience. It bridged the gap between theoretical knowledge and practical implementation in the domains of automation, embedded systems, and communication engineering. The Department expresses gratitude to **BMRCL officials** for their warm welcome and detailed technical sessions.

Photographs

Coordinator **HOD-ECE**

B.N.M Institute of Technology

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Department of Electronics & Communication Engineering

REPORT

Title	**Industrial Visit to DSedify**
Number of Students participated	**35**
Semester/Section	**7th semester ECE Students**
Date & Time	**4th July 2025 9:30 AM**
Staff Coordinators	• **Dr. Smitha Gayathri D, Associate Professor, ECE** • **Dr. Keerthi Kulkarni Associate Professor, ECE**
Organized Under	**IEEE CASS**

1. Introduction

An industrial visit to **DSedify Pvt. Ltd., Bengaluru** was organized for 7th semester students of the Department of Electronics and Communication Engineering, BNMIT. The visit was conducted under the aegis of the **IEEE Circuits and Systems Society (CASS), BNMIT Student Branch Chapter**. The objective was to expose students to the latest trends in skill-based learning, AI-powered training solutions, and career readiness programs.

2. About DSedify

DSedify Pvt. Ltd., a subsidiary of Dyashin Technosoft, is a forward-thinking company providing **AI-powered Learning as a Service (LaaS)**. The company's core mission is to bridge the gap between traditional academic education and industry expectations through customized, real-world, and certification-oriented training programs.

Motto of DSedify:

"Providing quality education, real-world skills, and hands-on learning in state-of-the-art facilities with expert mentors."

DSedify emphasizes both **technical and non-technical** skill development and supports learners through

campus, off-campus, and corporate training models tailored to ensure employability and career growth.

3. Key Highlights of the Visit

- **Tech Talks:** Students attended expert-led sessions focused on emerging technologies, industry trends, and career guidance — helping them stay ahead in interviews and on the job.
- **Internship Pathways:** DSedify detailed its structured internship offerings that connect academic learning with practical work environments — building real-world skills.
- **Workshops:** Hands-on project-based workshops were introduced, allowing students to collaborate, problem-solve, and innovate alongside industry professionals.
- **Campus Programs Presentation:**
    - **Campus Drives:** Enabling students to participate in placement opportunities with top companies.
    - **Industry Visits:** Providing direct exposure to industrial workflows and practices.
    - **Hackathons:** Encouraging creativity and technical excellence in competitive coding environments.
- **Experiential Learning:** The team at DSedify explained their commitment to **real-world project-based learning** through state-of-the-art labs, mentorship, and gamified learning tools for an engaging experience.

4. Student Learning Outcomes

From this visit, students gained:

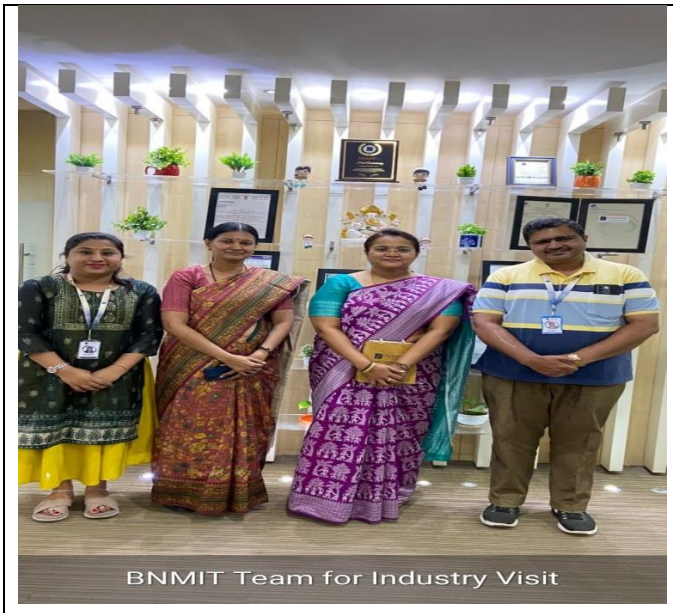
- First-hand exposure to an **AI-driven Learning Management System (LMS)**.
- Understanding of how **gamified and interactive learning platforms** enhance retention and engagement.
- Motivation to pursue **certification programs** and real-time project work.
- Insight into the soft skills, technical proficiency, and innovation mindset expected in modern workplaces.

5. Conclusion

The industrial visit to DSedify, facilitated by the IEEE CAS BNMIT chapter, was an enlightening experience for students. It provided a deep understanding of the evolving education-technology landscape and equipped students with the inspiration to become industry-ready professionals.

The Department of ECE extends its sincere appreciation to **DSedify Pvt. Ltd.** for their hospitality and to **IEEE CAS BNMIT** for making this visit possible.

Photographs



Students' Interaction from DSedify Team

Coordinator

HOD-ECE

B.N.M Institute of Technology

An Autonomous Institution under VTU, Approved by AICTE
Department of Electronics & Communication Engineering

REPORT

Title	Technical Talk on SoC & VLSI Industry Trends
Number of Students participated	100
Semester/Section	ECE Students
Date & Time	27th June 2025 11:30 AM
Staff Coordinators	• Dr. Yasha Jyothi M Shirur, HOD, ECE • Dr. Smitha Gayathri D, Associate Professor, ECE

Introduction

As part of the continuous effort to bridge the gap between academic learning and industrial advancements, a technical talk was organized in association with IEEE Circuits and Systems Society (CAS) and the IEEE Nanotechnology Council. The session was designed to provide students with deeper industry insights, particularly in the field of VLSI and semiconductor technology.

The session was delivered by **Mr. Santosh M S, SoC Functional Lead Validation Engineer at Intel**, a highly experienced Lead Validation Engineer with more than 10 years in the semiconductor domain, specializing in Pre and Post-silicon SoC functional validation. With a Master's degree in VLSI Design and Embedded Systems, Mr. Santosh has been instrumental in developing validation infrastructure and strategies for next-generation products.

Objectives of the Session

- To introduce students to System-on-Chip (SoC) architecture and functional validation processes.
- To provide insights into the latest trends and demands in the VLSI and semiconductor industries.
- To guide students on career opportunities and preparation strategies for entering the semiconductor domain.
- To help students understand the skill sets and industry tools required to excel in VLSI design and validation roles.
- To foster interactive learning by addressing student queries and clarifying doubts related to industry readiness.

Session Highlights

Mr. Santosh began the session by explaining the evolution and complexity of SoC designs, followed by a discussion on the current trends in the VLSI industry, including advanced node technologies, AI/ML in chip design, and increasing design validation challenges.

He then guided the students on how to:

- Build a strong foundation in digital electronics, HDL coding (Verilog/VHDL), and verification methodologies.
- Understand the role of internships, projects, and industry certifications in building employability.
- Prepare for technical interviews and transition successfully into core semiconductor roles.
- Develop both technical and soft skills, including problem-solving, debugging, communication, and teamwork.

The session concluded with an engaging Q&A segment, where Mr. Santosh clarified several student queries, making the talk highly interactive and impactful.

Conclusion

This technical talk proved to be an invaluable learning experience for the students. It successfully fulfilled its objectives by enhancing students' understanding of VLSI design, validation processes, and career-building strategies. The association with IEEE CAS and IEEE Nanotechnology Council added further credibility and visibility to the event, encouraging students to engage with professional societies and stay updated with technological advancements.

The session inspired many students to pursue further learning and specialization in the field of semiconductors and VLSI systems.

An engaging and insightful technical talk session by Mr. Santosh M S, Lead Validation Engineer, addressing 7th semester students on SoC design, VLSI industry trends, and career pathways in the semiconductor domain.

Group photo capturing the enthusiastic participation of 7th semester students and faculty members during the technical talk on “SoC & VLSI Industry Trends” by Mr. Santosh M S. The session, held on 27th June 2025 at BNMIT, was organized in association with the **IEEE BNM Institute of Technology Student Branch**, **IEEE Circuits and Systems Society (CAS)**, and the **IEEE Nanotechnology Council – Bangalore Section**. The event served as a great platform for knowledge sharing, industry insights, and student engagement in cutting-edge semiconductor technologies.

Coordinators HOD, ECE

B.N.M Institute of Technology

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Department of Electronics & Communication Engineering

REPORT

Title	Masterclass on Higher Education (Abroad Studies)
Number of Students participated	42
Semester/Section	7th semester ECE Students
Date & Time	26th June 2025, 11:00 AM – 12:00 PM
Staff Coordinators	• Dr. Yasha Jyothi M Shirur Prof. and HoD- ECE • Dr. Smitha Gayathri D, Associate Professor, ECE
Organized Under	IEEE CASS

Session Overview

The Masterclass on Higher Education (Abroad Studies) was organized to provide students with deep insights into global academic opportunities, application processes, and post-study prospects in leading international destinations. The session was conducted by experienced professionals from IDP Education, a global leader in international education services.

Speakers' Profile

Speaker Name	Designation	Organization	Speaker Profile
Tiru Mothukuri	Strategic Alliances Manager	IDP Education	Mr. Tiru has over 13 years of experience in the education sector. He has worked with leading companies like Pearson, People Combine, and Current, handling strategic alliances and partnerships with universities and colleges across South India, especially Bangalore.
Subhomoy Das	Designation Manager – USA	IDP Education	Mr. Subhomoy heads the team of counsellors at IDP Education who support students with end-to-end overseas education services, ensuring smooth academic transition and application processes.

Key Topics Covered

1. Global Academic Opportunities
2. End-to-End Application and Admission Process
3. Destination-wise details of major English-speaking countries: USA, UK, Australia, Canada, New Zealand, Ireland
4. Scholarship Opportunities available for students
5. Part-time Work Opportunities during study
6. Post-Study Work Opportunities in different countries
7. Interactive Q&A Session

About IDP Education

IDP Education is a global leader in international education services with a strong legacy of over 50 years. Headquartered in Australia, it is listed on the ASX and operates 130+ offices across 30+ countries.

• Co-owner of IELTS, the world's leading English language test recognized by 11,000+ organizations worldwide.

• Trusted partner of 800+ leading universities and institutions.

• Over 1,200 expert counsellors guiding students globally.

• Helped students secure admissions into 500,000+ courses, with one student placed every 14 minutes.

Services Offered to Students (at no cost):

- Counselling for courses and institutions
- Application submission and admission support
- Scholarship guidance
- Visa assistance and tuition fee payment support
- Pre-departure orientation & onshore student support

Conclusion

The masterclass successfully introduced students to the vast opportunities in overseas education and provided them with clarity on procedures, scholarships, and career pathways. The session not only inspired students to pursue global academic goals but also connected them with expert guidance through IDP Education.

IEEE-CASS Faculty Advisor
HOD-ECE,
BNMIT, Bengaluru

Vidyayāmruthamashnuthe

B.N.M. Institute of Technology

An Autonomous Institution under VTU

Department of Electronics & Communication Engineering

Internship Report on

Design Verification using System Verilog

Faculty Coordinators:

1. **Dr. Subodh Kumar Panda, Professor, Dept. of ECE, BNMIT**
2. **Dr. Vrunda Kusanur, Associate Professor, Dept. of ECE, BNMIT**

Number of students enrolled for the SDP: 64
Total number of hours conducted: 72

Trainers:
Cranes Varsity (Experts in Embedded Systems & Design, VLSI Design & Verification), Bengaluru.

Introduction

As part of the continuous effort to bridge the gap between academic learning and industrial advancements, a technical talk was organized in association with **IEEE Circuits and Systems Society (CASS) and the IEEE Nanotechnology Council**. The session was designed to provide students with deeper industry insights, particularly in the field of VLSI and semiconductor technology

Topics Covered during the Internship

Day	Date V Sem	Topics covered
Day1 6 Hrs.	02-06-2025	**Verilog Refresher & UART Design** – Modules, ports, operators – Behavioral vs. structural modeling
Day2 6 Hrs.	03-06-2025	**Verification Fundamentals** – Motivation for dedicated verification languages – Testbench architecture (TB, UUT, scoreboard)
Day3 6 Hrs.	04-06-2025	**SystemVerilog Data Types** – 2-state vs. 4-state – Strings, enums, events
Day4 6 Hrs.	05-06-2025	**Arrays, Queues & Collections** – Packed vs. unpacked arrays – Dynamic & associative arrays – Queue operations
Day5 6 Hrs.	06-06-2025	**Control Structures** – Loops (for, while, foreach) – Conditional statements (if, unique, case)
Day6 6 Hrs.	09-06-2025	**Tasks & Functions** – Void vs. automatic – Argument passing (input, output, ref)
Day7 6 Hrs.	10-06-2025	**Concurrency & IPC** – Fork–join variants (join, join_any) – Semaphores & mailboxes
Day8 6 Hrs.	11-06-2025	**OOP in SystemVerilog** – Classes, constructors, this – Inheritance, polymorphism – Virtual methods, encapsulation – Static vs. instance members
Day9 6 Hrs.	12-06-2025	**Constraint Randomization (Part 1)** – rand vs. randc – Basic constraints (inside, dist) – Soft constraints, inline constraints – Constraint precedence **Functional Coverage** – Covergroups, coverpoints, bins, cross coverage

Day10 6 Hrs.	13-06-2025	**SystemVerilog Assertions (SVA)** – Immediate vs. concurrent assertions – Sequences & properties
Day11 6 Hrs.	19-06-2025	**Practical Testbench Development** – Integrate coverage and assertions into a full testbench
Day12 6 Hrs.	20-06-2025	Mini-Project Implementation & Presentation

About the Program

Course Objectives:

- To master basic and advanced SystemVerilog Constructs
- To develop modular verification environments separating generator, driver, monitor, and checker to support code reusability and maintainability.
- To implement constrained randomization and functional coverage models (covergroups, bins, crosses) to measure test completeness.
- To write Systemverilog Assertions(SVA) for automatically detecting protocol violations.
- To apply all the techniques of Systemverilog to verify a standard IP block (e.g., UART), and implementing a mini-project.

Tools and Resources Used:

- EDAPlayground

Introduction:

The internship titled "**Design Verification Using SystemVerilog"** was conducted by Cranes Varsity, Bangalore from 2nd June 2025 to 20th June 2025 to 3rd year undergraduate students. This internship program was structured to provide a comprehensive journey from foundational Verilog concepts through advanced SystemVerilog features, concluded with a hands-on mini-project. This program exposed the students to not only theoretical concepts of hardware description and verification languages but also practical proficiency with real-world testbench architectures, coverage-driven verification, and assertion-based methodologies that are critical in modern VLSI design flows. The Quiz, assignments were conducted by the trainer to evaluate the understanding level of students during the internship.

Course Outcomes:

- To apply SystemVerilog data types, control structures, and object-oriented features to develop structured and reusable verification testbenches
- To implement functional coverage, constraint randomization, and assertions to validate digital designs and ensure verification completeness
- To develop and simulate end-to-end testbenches for standard protocols (UART, I2C, and SPI, integrating functional coverage and SVA for reliable design verification)

Topics Covered:

During the three-week internship on **Design Verification using SystemVerilog** conducted by Cranes Varsity, a wide range of essential topics in digital verification were systematically covered, starting from the fundamentals and progressing to advanced industry-relevant concepts. In the beginning of the internship, the studernts were introduced to Verilog, focusing on RTL design and simulation, using UART as a case study. Participants revisited core HDL concepts such as module creation, behavioral vs. structural modeling, and simulation waveform analysis. Building upon this foundation, the internship introduced the need for verification methodologies and testbench architectures, highlighting the roles of generators, drivers, monitors, scoreboards, and DUT interfaces.

As the internship progressed, the focus was on SystemVerilog-specific enhancements, starting with advanced data types including 2-state and 4-state variables, enumerations, strings, arrays, queues, and associative collections. During the internship, students explored control flow structures such as if-else, case, unique, and various loop constructs including for, while, and foreach. The internship also covered tasks and functions with detailed explanation of argument passing (input, output, ref) and automatic vs. static scoping. A significant portion of the program was dedicated to Object-Oriented Programming (OOP) in SystemVerilog, covering classes, constructors, encapsulation, inheritance, polymorphism, and virtual methods, enabling the creation of modular and scalable verification components.

The internship further explored constraint randomization**,** including rand and randc variables, inline and soft constraints, and the use of dist and inside constructs to influence value distribution. Functional coverage was introduced through covergroups, coverpoints, bins, and cross coverage,

allowing participants to measure test completeness and identify verification gaps. The concept of SystemVerilog Assertions (SVA) was another core highlight, where students learned to write immediate and concurrent assertions, define sequences and properties, and integrate them into testbenches for protocol and timing checks.

All of these concepts were discussed through hands-on coding sessions using tools such as EDA Playground. The internship concluded with a comprehensive mini-project where participants applied everything learned to verify a standard protocol (e.g., UART or I2C), implementing layered testbenches, randomized testing, coverage collection, and assertion-based validation. Overall, the internship offered a complete learning experience in modern digital design verification practices using SystemVerilog.

Students were given with quiz at the end of the course and evaluated using Google Classroom.

Figure 1(a)

Figure 1(b)

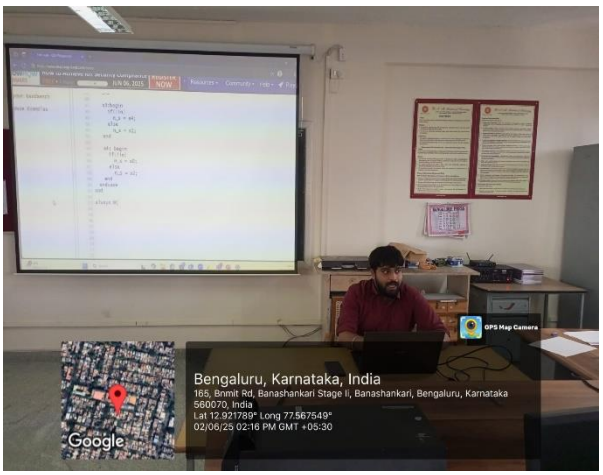

Figure 1(c)

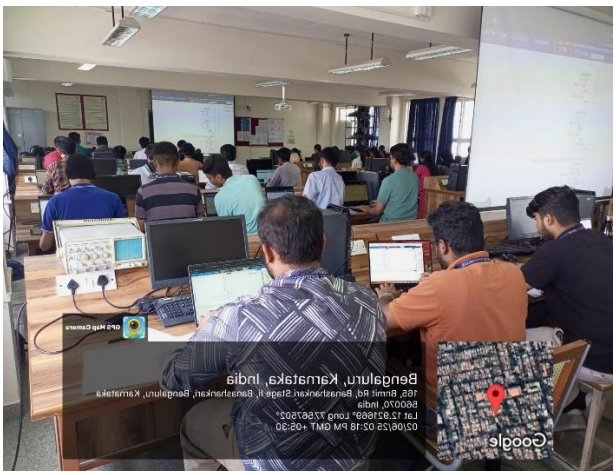

Figure 1(d)

Figure 1: Student Interaction during Internship

Yashajyothi

HOD, ECE

B.N.M Institute of Technology

An Autonomous Institution under VTU, Approved by AICTE
Department of Electronics & Communication Engineering

REPORT

Title	**Avinya 2025 – Project Exhibition**
Number of Students participated	**120**
Semester/Section	**ECE Students**
Date & Time	**12th April 2025 9:30 AM**
Staff Coordinators	• **Dr. Ashwini Savanth, Associate Professor, Dept. of ECE** • **Dr. Sujaya B. L., Associate Professor, Dept. of ECE** • **Dr. Smitha Gayathri D, Associate Professor, ECE**

B. N. M. Institute of Technology

An Autonomous Institution under VTU.

27th Cross, 12th Main, Banashankari 2nd Stage, Bengaluru 560 070.

Department of Electronics & Communication Engineering

Avinya 2025

12th April 2025

Project Exhibition

In Association with

The Institution of Engineers (INDIA)

IEEE Communications Society

IEEE Nanotechnology Council

IEEE Circuits and Systems Society

Venue : N 505 New Building

Time : 9:30am

Convenors

Dr. Yasha Jyothi M. Shirur
Professor. & HoD,
Dept of ECE

Dr. Bindu S
Professor,
Dept of ECE

Co-ordinators

Dr. Ashwini Savanth
Associate Professor,
Dept of ECE

Dr. Sujaya B L
Associate Professor,
Dept of ECE

Sri. Narayan Rao R. Maanay
Chairman GB
BNMIT

Prof. T. J. Rama Murthy
Director
BNMIT

Dr. S. Y. Kulkarni
Additional Director &Principal
BNMIT

Prof. Eishwar N. Maanay
Dean
BNMIT

Dr. Krishnamurthy G. N.
Deputy Director
BNMIT

The Department of Electronics and Communication Engineering at B.N.M. Institute of Technology (BNMIT), Bengaluru, hosted its annual **Project Exhibition – Avinya 2025** on 12th April 2025. The event was a significant platform for final-year undergraduate students to showcase their innovative project work, aligning with the latest trends and technologies in the domain of electronics and communication engineering.

- **Objective of the Event**

The core objective of **Avinya 2025 – Project Exhibition** was to provide a dynamic platform for final-year undergraduate students of the **Department of Electronics and Communication Engineering (ECE)** at BNMIT to demonstrate their technical expertise, innovative thinking, and project execution capabilities. It served as a capstone to their academic journey, enabling them to bridge the gap between theoretical knowledge and practical implementation.

The event was meticulously designed to achieve the following key goals:

Promote Innovation and Creativity:

Avinya encouraged students to ideate, design, and develop original solutions to contemporary problems. Students were motivated to think beyond conventional classroom learning and explore new technological domains such as IoT, AI, embedded systems, VLSI, and smart communication systems.

Enhance Practical and Technical Skills:

By building and showcasing real-world projects, students honed their engineering skills in circuit design, coding, hardware-software integration, simulation, and debugging. This hands-on experience is essential for reinforcing theoretical concepts learned during their course of study.

Foster Research and Analytical Thinking:

The event emphasized analytical and research-oriented thinking. Students undertook detailed literature reviews, problem analysis, and solution design to develop technically sound and meaningful projects.

Encourage Teamwork and Collaboration:

Project-based learning at Avinya promoted teamwork, with students working in groups to manage various aspects of the project—planning, execution, testing, and presentation. This nurtured their communication, leadership, and interpersonal skills.

Expose Students to Industry Standards:

With associations from IEEE societies and evaluation by industry experts, Avinya provided insights into industry expectations and emerging trends. It gave students an opportunity to receive constructive feedback from seasoned professionals, helping them align their work with current industry standards.

Develop Entrepreneurial and Problem-Solving Mindsets:

Many of the projects had practical and societal applications, pushing students to develop solutions with real-world impact. This fostered an entrepreneurial spirit and encouraged them to consider how their innovations could evolve into startups or products.

Build Confidence and Communication Skills:

Presenting their work in front of faculty, peers, and external evaluators helped students gain confidence and improve their communication and presentation abilities—skills vital for both professional and academic growth. In essence, **Avinya 2025** was not just a project exhibition—it was a celebration of student innovation, a reflection of quality education, and a launchpad for future technologists, researchers, and entrepreneurs. It reaffirmed BNMIT's commitment to nurturing well-rounded, industry-ready engineering graduates.

- **Collaboration and Associations**

  Avinya 2025 was organized in association with prestigious professional bodies:

  IEEE Communication Society (ComSoc)

  IEEE Nanotechnology Council

  IEEE Circuits and Systems Society (CAS)

  The Institution of Engineers (India) – IEI

  The support of these organizations added technical value and credibility to the event and helped in establishing industry-academia linkage.

- **Inauguration and Event Highlights**

  The event commenced at 9:30 AM in Room N 505 of the New Building at BNMIT. The inauguration was graced by key dignitaries:

  Sri. Narayan Rao R. Maanay, Secretary, BNMIT

  Prof. T.J. Rama Murthy, Director, BNMIT

  Dr. S. Y. Kulkarni, Advisor & Principal, BNMIT

  Prof. Eishwar N. Maanay, Dean, BNMIT

  Dr. Krishnamurthy N. M., Deputy Director, BNMIT

  The dignitaries emphasized the importance of applied learning and project-based education. They encouraged students to explore entrepreneurial possibilities through their innovations.

- **Project Themes and Student Participation**

  The exhibition featured a diverse range of projects from final-year ECE students. The projects spanned across domains such as:

  Embedded Systems

  VLSI Design

  Signal Processing

  IoT and Smart Devices

  Wireless Communication

  AI and Machine Learning Applications in ECE

  Robotics and Automation

Each project was evaluated by a panel comprising industry experts and faculty members based on criteria like innovation, technical complexity, societal impact, and presentation.

- **Evaluator Panel**

The evaluation of student projects was enriched by the presence of eminent industry professionals, whose experience and domain knowledge brought practical relevance to the event. The evaluators were:

- **Mr. Mayur Kulkarni**

  Designation: Divisional Manager

  Organization: Engine R&D, Ashok Leyland, Hosur

  Area of Specialization: Engine Development and Calibration

- **Dr. Narendra Kumar**

  Organization: GTTC, Bengaluru

- **Mr. Mahesh Devgiri**

  Industry Expert

These evaluators provided insightful suggestions, highlighted areas for improvement, and inspired students to think beyond academic boundaries.

- **Coordination and Organization**

The success of Avinya 2025 was driven by the meticulous efforts of the event team. The convenors of the event were:

Dr. Yasha Jyothi M. Shirur, Professor & HoD, Dept. of ECE

Dr. Bindu S., Professor, Dept. of ECE

The coordination team included:

Dr. Ashwini Savanth, Associate Professor, Dept. of ECE

Dr. Sujaya B. L., Associate Professor, Dept. of ECE

Dr. Smitha Gayathri D, Associate Professor, Dept. of ECE

Their leadership ensured smooth execution and a vibrant academic atmosphere throughout the day.

- **Conclusion**

Avinya 2025 turned out to be a remarkable event that not only highlighted the technical proficiency of students but also nurtured their ability to address real-world challenges using engineering principles. The event fostered a spirit of innovation and served as a stepping stone for students aspiring to pursue research, higher education, or careers in the industry.

The Department of Electronics and Communication Engineering at BNMIT continues its legacy of excellence by organizing such impactful events, further strengthening its commitment to holistic and experiential education.

Group photo of dignitaries, faculty, and student participants of Avinya 2025, celebrating innovation and collaboration in engineering.

Students enthusiastically explain the project to a judge during the Avinya 2025 exhibition, showcasing innovation and technical skills.

Coordinators HOD, ECE