

B.N.M. Institute of Technology

An Autonomous Institution under VTU
Dept. of Electronics and Communication Engineering
M. Tech (VLSI Design and Embedded Systems)

Semester: I

Course Name: Custom IC DESIGN

Course Code: 25VDE211

L: T: P: J	4: 0: 0: 0	CIA Marks: 50
Credits:	4	SEA Marks: 50
Hours	50	SEA Duration: 03 Hours

Pre-Requisites: A Brief History of MOS Transistors, Theory and Fundamentals of Integrated Circuits, Logic Design, Basic of delay calculation and storage elements

Course Learning Objectives: The students will be able to

1	Explore the concepts of Custom IC design flow and CMOS logic cells
2	Understand the Custom IC Library Design and Programmable ASIC logic cells
3	Explore the basics of Physical Design techniques in Custom IC Design
4	Present the overview of routing techniques in Custom IC Design
5	Understand the basics of CHIPLETS

Module-1: Introduction to Custom IC Design	No. of Hours	Blooms Cognitive Levels
<p>Types of ASICs: Full Custom ASIC, Semi- custom based ASICs, Standard Cell based ASIC, Gate array-based ASIC, Channeled gate array, Channel less gate array, Structured gate array, Programmable logic devices, FPGA, ASIC Design flow.</p> <p>CMOS Logic: Data path Logic Cells: Data Path Elements, Adders: Carry skip, Carry bypass, Carry save, Carry select, Conditional sum, Multiplier (Booth encoding), Data path Operators, I/O cells, Cell Compilers.</p>	10	Apply CO1
Module-2: ASIC Library Design and Programmable ASIC Logic Cells		
<p>Logical Effort: Predicting delay, Logical area and logical efficiency, Logical paths, Multistage cells, optimum delay, optimum number of stages. Library-cell design.</p> <p>Programmable ASIC Logic Cells: MUX as Boolean function generators, Shannon's expansion theorem, Actel ACT: ACT 1, ACT 2 and ACT 3 Logic Modules, Xilinx LCA: XC3000 CLB, Altera FLEX and MAX, Programmable ASIC I/O Cells: Xilinx and Altera I/O Block.</p>	10	Apply CO2
Module-3: ASIC Physical Design: Partitioning, Floor Planning and Placement		
<p>ASIC Construction: Physical Design, CAD Tools System partitioning, Estimating ASIC size.</p> <p>Partitioning: Goals and objectives, Constructive Partitioning, Iterative Partitioning Improvement, KL, FM and Look Ahead algorithms.</p> <p>Floor planning and placement: Goals and objectives, Measurement of delay in Floor planning, Floor planning tools, Channel definition, I/O and Power planning and Clock planning.</p> <p>Placement: Goals and Objectives, Min-cut Placement algorithm, Iterative Placement Improvement, Time driven placement methods, Physical Design Flow.</p>	10	Apply CO3
Module-4: ASIC Physical Design: Routing Techniques		
<p>Global Routing: Goals and objectives, Global Routing Methods, Global routing between blocks, Back annotation.</p> <p>Detailed Routing: Goals and objectives, Measurement of Channel Density, Left-Edge Algorithm, Area-Routing Algorithms, Multilevel routing, Timing -Driven detailed routing, Final routing steps, Special Routing, Circuit extraction and DRC.</p>	10	Apply CO4

Yashraj

G

Additional Director
BNM Institute of Technology
Bangalore

Module-5: Introduction to CHIPLETS		
Introduction to Chiplet technology, Commercial Challenges: Business and Technical, Interface Challenges, D2D Interface Types: Serial vs Parallel, Proprietary vs Open D2D Standards, Packaging Innovations for Chiplets, Chiplet Security Challenges: Proving and Securing Authenticity, Silicon-Based Countermeasures, Supply Chain Security & Provisioning.	10	Understand CO5

Course Outcomes: After completing the course, the students will be able to	
25VDE211.1	Design the data path elements for ASIC cell libraries and understand the concepts of ASIC design methodology
25VDE211.2	Design the Mux-based logic cells and compute the Logical effort of a single stage network and Multistage network
25VDE211.3	Apply the concepts of Partitioning, Floor planning, and Placement techniques in Custom IC Design
25VDE211.4	Apply the concepts of Global and Detailed routing techniques in Custom IC Design
25VDE211.5	Explore the various opportunities and challenges in the area of CHIPLETS
25VDE211.6	Design and implement a Custom IC for a specific application.

Reference Books	
<ol style="list-style-type: none"> 1. Application - Specific Integrated Circuits, Michael John Sebastian Smith Addison- Wesley Professional, 2015. 2. CMOS VLSI Design: A Circuits and Systems Perspective Neil H.E. Weste, David Harris, and Ayan Banerjee, Addison Wesley/ Pearson education 3rd edition, 2011. 3. VLSI Design: A Practical Guide for FPGA and ASIC Implementations, Vikram Arkalgud Chandrasetty, Springer, ISBN: 978-1-4614-1119-2. 2011. 4. An ASIC Low Power Primer, Rakesh Chadha, Bhasker J Springer, ISBN: 978-14614-4270-7. 5. Heterogeneous Integration-CHIPLETS, White Paper, https://www.gsaglobal.org/wp-content/uploads/2023/02/2022-IPIG-Heterogenous-Integration-Chiplets-White-Paper-Final-v4.pdf, 2022. 6. The March Towards Chiplets, Ed Sperling and Karen Heyman, Semiconductor Engineering December 15, 2022. https://semiengineering.com/the-march-toward-chiplets/. 	

Marks Distribution for Assessment:

PCC	CIA	SEA	CIA (50)			SEA Conduction: 100 M Reduced to: 50 M
				I	II	
Conduction	50	50	Written Test	50	50	Five questions with each of 20 marks (with internal choice). Student should answer one full question from each module
				Average of two tests – 25 Marks		
			Assignment	15		
			AAT	10		

B.N.M. Institute of Technology

An Autonomous Institution under VTU
 Dept. of Electronics and Communication Engineering
 M. Tech (VLSI Design and Embedded Systems)

SEMESTER – I

Course Name: QNX based Embedded RTOS Design

Code: 25VDE212

L: T:P: J	2:0:4:0	CIA Marks: 50
Credits:	4	SEA Marks: 50
Hours	50	SEA Duration: 03 Hours

Course Learning Objectives:

This course will enable students to

- Understand the Architecture of QNX Neutrino RTOS and Develop Real-Time Applications
- Understand the working of QNX Development Tools (Momentics IDE)
- Able to Implement Process and Thread Management
- Understand the Master Inter-Process Communication (IPC)
- Debug and Optimize Embedded Systems

Pre-Requisites: Operating Systems basics and C programming and Linux commands.

QNX Momentics Development Basics: Eclipse Basics, Targets, Projects and Source, Compiling, Exercise, Running and Debugging, Exercise and Versions.

QNX Neutrino RTOS Environment Setup

Objective: Install and configure QNX SDP, Momentics IDE, and target system (real or virtual).

Outcome: Understand development workflow in QNX.

	Number of Hours	Bloom's Level
--	-----------------	---------------

Module-1

Introduction to QNX Real Time Operating System: Architecture – Executive, Microkernel, Inter process Communication, Processes and Threads model, Timing, Interrupt Handling, Scheduling, Boot Sequence, Security.

4

Apply (CO1)

Laboratory Component: Process Creation and Management

Running and Debugging: Exercise

Objective: Create and run hello world example on VM Ware virtual machine or Rasp-pi board.

Outcome: Print hello world on panel of QNX Momentics IDE

Objective: Write a program to create and manage multiple processes.

Outcome: Demonstrate use of fork(), exec(), and wait() in QNX.

6

Apply (CO1, CO2)

Self-Study Component: Demonstrate how to Detect the termination of a child processes.

Module-2

Security Policies: Introduction to the use of security policies in securing a QNX system, Process Managers: System Library, Shared Objects, OS Services, Boot Sequence and Security.

4

Apply (CO2)

<p>Processes, Threads & Synchronization: Introduction, Processes: Creation and Detecting termination, Threads, Process Termination and Cleanup,</p>		
<p>Laboratory Component: Thread Creation and Synchronization Processes - Detecting Termination: Exercise Synchronization - Mutexes: Solution to synchronization problems using Mutex Synchronization - Conditional Variables: Program in synchronization using Conditional Variables.</p> <p>Self-Study Component: Synchronization - Atomic Operations: Simple program solutions on atomic operations</p>	6	Apply (CO2)
Module-3		
<p>Introduction to QNX Inter-Process Communication: Message Passing, Designing a Message Passing System (1): Pulses, Client Information Structure, How a Client Finds a Server, Multi-Part Messages.</p>	4	Understand (CO3)
<p>Comparing QNX IPC Methods: The Methods, How to Choose.</p>		
<p>Laboratory Component: Inter-Process Communication using Message Passing: Implement server-client IPC using MsgSend(), MsgReceive(), and MsgReply(). Programs to demonstrate IPC with pulses Programs to demonstrate IPC with multipart messages</p> <p>Self-Study Component: Assignment on Inter-Process Communication (IPC)</p>	6	Apply (CO3, CO4)
Module-4		
<p>QNX Inter-Process Communication: Issues Related to Priorities, Designing a Message Passing System (2): Event Delivery Shared Memory</p> <p>Introduction to Hardware Programming: Hardware I/O, Programming PCI bus devices, Handling Interrupts.</p>	4	Apply (CO4)
<p>Laboratory Component: Event Delivery: Program to demonstrate IPC – event delivery Shared Memory: Implement IPC using shared memory</p> <p>Self-Study Component: Handling Interrupts : Program on Interrupt handling</p>	6	Apply (CO4)
Module-5		
<p>Timers, Clocks and Timeouts: Introduction, Timing Architecture, Getting and Setting the System Clock, Introduction to Timers, High-Resolution Timers, Design Considerations, Kernel Timeouts.</p> <p>Build a QNX Neutrino Boot/OS Image: Introduction, Images & Buildfiles, Images & Buildfiles: Exercise option</p>	4	Apply (CO5)

Resource Managers: Introduction, A Simple Resource Manager: Initialization and Handling read() and write().		
Laboratory Component: Timers: Program on timers Program to initialize Resource managers. Handling read() and write() - read()	6	Apply (CO5)
Self-Study Component: Implementation of Image building		
Course outcomes: The students will be able to <ul style="list-style-type: none"> • Understand the Architecture of QNX Neutrino RTOS and implement Real-Time Applications • Apply the working of QNX Development Tools (Momentics IDE) on Processes, Threads & Synchronization. • Implement the QNX Inter-Process Communication and compare QNX IPC Methods • Apply the QNX Inter-Process Communication with Hardware Programming and Interrupt handling • Understand the timing architecture, High-Resolution Timers, Images & Buildfiles and Resource Manager 		
Reference Books: <ol style="list-style-type: none"> 1. Operating Systems: Three easy pieces - Remzi H. Arpaci-Dusseau, Andrea C. Arpaci-Dusseau, Books, LLC, 2018 2. The Linux Programming Interface- Michael Kerrisk, No Starch Press, 2010 3. Operating Systems: Design and Implementation - Andrew S Tanenbaum, Pearson/Prentice Hall, 2006 		

Marks Distribution for Assessment

CIA (50)	Components	Description	Marks
	Written test	<ul style="list-style-type: none"> • Total Number of Test:02 • Each Theory test will be conducted for 30 marks • Average of 2 tests= 30 Marks 	30
	Practical	<ul style="list-style-type: none"> • Total number of Test: 02 [Part-A (Module-1 and 2) and Part-B (Module 3,4 and 5)] Each Lab test will be conducted for 50 marks and reduce to 10 Average of 2 tests= 10 Marks • Laboratory conduction is to be evaluated every week. conducted & Viva = 5 Marks Lab Record = 5 Marks 	10
		Total CIA	50
SEA (50)	Practical Exam	<ul style="list-style-type: none"> • Students are allowed to pick one experiment from Part-A and one experiment from PART-B. Mark Distribution: Total 100 marks Part – A: 40 Marks (Procedure:6, Execution:28, Viva: 6) Part – B: 60 Marks (Procedure:9, Execution:42, Viva: 9) Scaled down to 50 marks 	50
		Total Marks for the Course	100

B.N.M. Institute of Technology

An Autonomous Institution under VTU
Dept. of Electronics and Communication Engineering
M. Tech (VLSI Design and Embedded Systems)

Semester: I

Course Name: Modern CMOS Circuit Design Course Code: 25VDE213

L: T: P: J	3: 0: 2: 0	CIA Marks: 50
Credits	4	SEA Marks: 50
Hours/Week (Total)	5 (50)	SEA Duration: 03 Hours

Pre-Requisites: Metal Oxide Semiconductor (MOS) Structure, Inverters, Semiconductor memory, Concept of Pass Transistor and BJTs.

Course Learning Objectives: The students will be able to

1	Explain VLSI Design Methodologies
2	Learn Static and Dynamic operation principles, analysis and design of inverter circuit.
3	Infer state of the art Semiconductors Memory circuits.
4	Outline the comprehensive coverage of Methodologies and Design practice that are used to reduce the Power Dissipation of largescale digital circuits.
5	Illustrate VLSI and ASIC design

Module-1: MOS Transistor and MOS Inverters- Static Characteristics	No. of Hours	Blooms cognitive Levels
MOS Inverters-Static Characteristics: Introduction, Resistive-Load Inverter, Inverters with n-Type MOSFET Load. CMOS Inverter. Scaling and Small-Geometry Effects. Lab Experiment: 1	10	Apply CO1
Module-2: MOS Inverters:		
Switching Characteristics and Delay-Time Definition, Calculation of Delay Times, Inverter Design with Delay Constraints, Estimation of Interconnect Parasitics, Calculation of Interconnect Delay, Switching Power Dissipation of CMOS Inverters. Lab Experiment: 2 & 3	10	Analyze CO2
Module-3: Semiconductor Memories:		
Dynamic Random Access Memory (DRAM), Static Random Access Memory (SRAM), Nonvolatile Memory, Flash Memory & Ferroelectric Random Access Memory (FRAM) Lab Experiment: 4 & 5	10	Apply CO3
Module-4: BiCMOS and Dynamic Logic Circuits		
Dynamic Logic Circuits: Basic Principles of Pass Transistor Circuits, Voltage Bootstrapping, Synchronous Dynamic Circuit Techniques, High Performance Dynamic CMOS circuits. BiCMOS Logic Circuits: Structure and Operation, Dynamic Behavior of BJTs: Basic BiCMOS Circuits: Static Behavior and BiCMOS Applications Lab Experiment: 6 & 7	10	Apply CO4
Module-5: Overview of FinFET Device Technology		
Introduction to FinFET, FinFET Devices for VLSI Circuits and Systems, A Brief History of FinFET Devices, Construction and working of FinFET, FinFET Manufacturing Technology, Bulk-FinFET Fabrication, SOI-FinFET Process Flow. Lab Experiment: 8 to 10	10	Apply CO4

Yashraj

Lab Experiments

1. Draw NMOS characteristics and Determine
 - i. Cut-Off Region
 - ii. Ohmic or Linear Region
 - iii. Saturation Region
2. a. Design an **Inverter** with given specifications, completing the design flow mentioned below:
 - a. Draw the schematic and verify the following
 - i. DC Analysis
 - ii. Transient Analysis
 - b. Draw the Layout and verify the DRC, check for LVS Extract RC and back annotate the same and verify the Design Verify & Optimize for Time, Power and Area to the given constraint
3. a. Draw **CMOS inverter with load capacitance** of 0.1pF and set the widths of inverter with $W_n = W_p$, $W_n = 2W_p$, $W_n = W_p/2$ and length at selected technology. Carry out the following
 - i. Set the input signal to a pulse with rise time, fall time of 1ns and pulse width of 10ns and time period of 20ns and plot the input voltage and output voltage of designed inverter.
 - ii. From the simulation results compute t_{pHL} , t_{pLH} and t_d for all three geometrical settings of width.
 - iii. Tabulate the results of delay and find the best geometry for minimum delay for CMOS inverter
 - b. Draw layout of inverter with $W_p/W_n = 40/20$, use optimum layout methods. Verify for DRC and LVS, extract parasitic and perform post layout simulations, compare the results.
4. Design of Dynamic CMOS Logic, $Y = AB + C$
5. Design of Domino CMOS Logic, $Y = (A+B) * C$
6. Draw the schematic of 2- input CMOS NAND gate having similar delay as that of CMOS inverter computed in experiment 2. Verify the functionality of NAND gate and also find out the delay t_d for all four possible combinations of input vectors. Table the results. Increase the drive strength to 2X and 4X and tabulate the results.
 - b. Draw layout of NAND with $W_p/W_n = 40/20$, use optimum layout methods. Verify for DRC and LVS, extract parasitic and perform post layout simulations, compare the results.
7. a. Draw the schematic of Buffer using inverter and verify the simulation.
 - b. Draw layout of BUFFER circuit, verify for DRC and LVS, extract parasitic and perform post layout simulations, compare the results.
8. Draw the schematic of TRI State INVERTER and TRI State Buffer using MOSFETs and verify the simulation. Draw layout and verify for DRC and LVS, extract parasitic and perform post layout simulations, compare the results.
9. a. Draw the schematic of D-latch using inverter and verify the simulation.
 - b. Draw layout of D-latch circuit, verify for DRC and LVS, extract parasitic and perform post layout simulations, compare the results.
10. a. Draw the schematic of D FF using gates and verify the simulation.
 - b. Draw Layout of D FF Verify for DRC and LVS, extract parasitic and perform post layout simulations, compare the results.

Course Outcomes: After completing the course, the students will be able to	
25VDE213.1	Apply the design concepts to MOS inverters and CMOS inverters by understanding their static characteristics. Evaluate the effects of scaling and small-geometry devices on inverter performance for optimized digital circuit design
25VDE213.2	Analyze the Switching Characteristics in Digital Integrated Circuits.
25VDE213.3	Apply concepts study memory behavior and performance.
25VDE213.4	Apply the design concepts to evaluate BiCMOS and dynamic logic circuits.
25VDE213.5	Understand the structure, working, and applications of FinFET devices in VLSI circuits. Analyze FinFET manufacturing technologies, including Bulk and SOI process flows, for modern semiconductor design
25VDE213.6	Apply design concepts to analyze MOS, CMOS, BiCMOS, dynamic logic circuits, and FinFET devices to optimize VLSI circuit performance

Reference Books	
1.	Sung Mo Kang & Yusuf Leblebici, "CMOS Digital Integrated Circuits: Analysis and Design", Tata McGraw-Hill, Third Edition.
2.	FinFET Devices for VLSI Circuits and Systems, Samar K. Saha, Taylor and Francis Group, 2020.
3.	Neil Weste and K. Eshragian, "Principles of CMOS VLSI Design: A System Perspective", Second Edition, Pearson Education (Asia) Pvt. Ltd. 2000.
4.	Wayne, Wolf, "Modern VLSI Design: System on Silicon" Prentice Hall PTR/Pearson Education, Second Edition, 1998.
5.	Douglas A Pucknell & Kamran Eshragian, "Basic VLSI Design" PHI 3rd Edition (original Edition – 1994).

Assessment Process

Professional Core with Integrated Lab (PCI) – Course with Lab

PCI	CIA	SEA	CIA (50)		SEA Conduction: 100 M Reduced to: 50 M	
			I	II		
Conduction	50	50	Written Test	50	50	Five questions with each of 20 marks (with internal choice). Student should answer one full question from each module
			Assignment	Average of two tests – 50 marks scaled down to 15 marks		
			Practical	Average of 2 Assignments – 10M		
			Weekly Assessment – 10 Marks IA test – 15 Marks (IA test to be conducted for 50 M and scaled down to 15M)			
			Total – 50 Marks		Total – 50 Marks	

B.N.M. Institute of Technology

An Autonomous Institution under VTU
Dept. of Electronics and Communication Engineering
M. Tech (VLSI Design and Embedded Systems)

Semester: I

Course Name: System Verilog for Design and Verification		Course Code: 25VDE214
L: T: P: J	2: 0: 2: 2	CIA Marks: 50
Credits:	4	SEA Marks: 50
Hours	50	SEA Duration: 03 Hours

Pre-Requisites: Basics understanding of combinational and sequential logic circuits, Basics of C and C++ language, Knowledge about Simulation, Verilog HDL concepts and programming

Course Learning Objectives: The students will be able to

1	Understand digital system verification using object oriented methods.
2	Learn the System Verilog language for digital system verification.
3	Create/build test benches for the basic design/methodology.
4	Use constrained random tests for verification.
5	Understand concepts of Interprocess communication and functional coverage.

Module-1: Data Types and Verification Guidelines	No. of Hours	Blooms Cognitive Levels
<p>Data Types : Built in data types, Fixed Size Arrays, Dynamic Arrays, Queues, Associative Arrays. Array Methods, Creating New Types with typedef, Enumerated Types, Tasks, Functions, and Void Functions</p> <p>Verification Guidelines: The verification process, directed testing, constrained random stimulus, randomization, test bench components, layered testbench.</p> <p>Lab Experiment:</p> <ul style="list-style-type: none"> • Develop a System Verilog code to demonstrate two-state and four-state data types. • Write a program to create an array (Fixed Array an Dynamic Array) of objects in System Verilog. <p>Develop a System Verilog code to demonstrate push_front, pop_front, with respect to Queues.</p>	10	Apply CO1
<p>Module-2: Connecting the test bench and design & OOP Concepts</p> <p>Connecting the test bench and design Separating the test bench and design, The interface construct, System Verilog assertions.</p> <p>OOP Concepts Introduction, Your First Class, Where to Define a Class, OOP Terminology, Creating New Objects, Object Deallocation, Using Objects, Static Variables vs. Global Variables, Class Methods, Defining Methods Outside of the Class, Scoping Rules</p> <p>Lab Experiment:</p> <ul style="list-style-type: none"> • Demonstrate Full adder using System Verilog with 'Interface' construct. • Develop a System Verilog code to demonstrate classes. 	10	Apply CO2
Module-3: Randomization		

M. S. R. Prasad

G

Additional Director & Principal
BNM Institute of Technology
Bangalore - 560070

<p>Introduction, Randomization in System Verilog, Constraint details, Solution probabilities, Valid constraints, In-line constraints, Random number functions, Common randomization problems, Random control, Random Number Generators.</p> <p>Lab Experiment:</p> <ul style="list-style-type: none"> • Write a program to demonstrate the difference between 'rand' and 'randc'. • Write a program to demonstrate weighted random distribution with dist. 	10	Apply CO3
Module-4: Threads and Interprocess Communication		
<p>Working with Threads, Disabling Threads, Events, Semaphores, Mailboxes</p> <p>Lab Experiment:</p> <ul style="list-style-type: none"> • Write a program to demonstrate access control using semaphore for one/multiple key. • Write a program to demonstrate Mailbox uses in interprocess communication. 	10	Apply CO4
Module-5: Functional Coverage		
<p>Coverage types, Coverage strategies, Simple coverage example, Anatomy of Cover group and Triggering a Cover group, Data sampling, Cross coverage, Generic Cover groups, Coverage options, Analyzing coverage data, measuring coverage statistics during simulation.</p> <p>Lab Experiment:</p> <ul style="list-style-type: none"> • Demonstrate 4-bit adder with the verification environment • Write a System Verilog code to declare explicit Bins. 	10	Apply CO5

Projects:

1. Verification of Vedic Multiplier using System Verilog.
2. Verification of Convolutional Encoder and Viterbi Decoder using System Verilog.
3. Verification of Signed integer divider using System Verilog.
4. Verification of Wallace Tree Multiplier using System Verilog.
5. Design and verify a UART with configurable baud rate using System Verilog.

Course Outcomes: After completing the course, the students will be able to	
25VDE214.1	Apply SystemVerilog features(data types, arrays, and queues) to develop digital systems and verify using directed and randomized testing.
25VDE214.2	Implement object-oriented programming, interfaces, and assertions in SystemVerilog for efficient testbench development and verification.
25VDE214.3	Use SystemVerilog's randomization constructs(constraints, control options, and random number) utilities to enhance verification efficiency and coverage.
25VDE214.4	Apply SystemVerilog constructs (threads, events, semaphores, and mailboxes) to implement concurrent verification processes.
25VDE214.5	Evaluate the effectiveness of functional coverage and interprocess synchronization techniques in complex verification scenarios.

Reference Books

1. Chris Spear, 'System Verilog for Verification – A guide to learning the Test bench language features', Springer Publications, 3rd Edition, 2012.
2. Stuart Sutherland, Simon Davidmann, Peter Flake, "System Verilog for DesignA guide to using system verilog for Hardware design and modeling", Springer Pulications, 2nd Edition, 2008.
3. Janick Bergeron, "Writing Testbenches Using SystemVerilog", 1st Edition, Springer Publications, 2010.
4. Janick Bergeron, Eduard Cerny, Alan Hunter, and Andy Nightingale, "Verification Methodology Manual for SystemVerilog", Springer Pulications, 2014.

Marks Distribution for Assessment:

PBL	CIA	SEA	Academic Year 2023-24		
			CIA (50M) T-Theory; E- Execution M-Marks		
Conduction	50M	50M		IA -1 (40M)	IA-2(40M)
			IA TEST	20(T) + 20(E)	20(T) + 20(E)
			Continuous Assessment	Weekly Assessment (Project/record) 5+5=10M	
			TOTAL	40+10= 50M	
SEA(Project)	-	Project assessed for 100 marks reduced to 50 marks	Conduction :100 marks Reduced to :50 marks	<ul style="list-style-type: none"> • Write up - 10M • Project report – 25M • Presentation and Documentation - 50M • Viva Voce – 15M 	
			TOTAL	50M	

B.N.M. Institute of Technology

An Autonomous Institution under VTU
Dept. of Electronics and Communication Engineering
M. Tech (VLSI Design and Embedded Systems)

Semester: I

Course Name: Hybrid AI models for Power Efficient VLSI system Course Code: 25VDEP2151

L: T: P: J	3 :0 :0 :0	CIA Marks: 50
Credits:	3	SEA Marks: 50
Hours/Week (Total)	3	SEA Duration: 03 Hours

Pre-Requisite : Basic knowledge of Digital Electronics, CMOS Design, and introductory Machine Learning

Course Learning Objectives: The students will be able to

- 1 To introduce and understand the fundamentals of AI and its relevance to VLSI design.
- 2 To explore hybrid AI models combining various AI techniques for power optimization in VLSI systems.
- 3 To analyze power estimation and reduction techniques using AI methodologies.
- 4 To provide hands-on experience with tools and frameworks applicable to AI-driven VLSI design.
- 5 To evaluate case studies demonstrating the application of hybrid AI models in real-world VLSI systems.

Module 1: Introduction to AI in VLSI Design	No. of Hours	Blooms Cognitive Levels
Overview of AI techniques: Machine Learning, Deep Learning, Fuzzy Logic, Genetic Algorithms, Relevance of AI in VLSI design and power optimization, Challenges in traditional VLSI design methodologies, Introduction to hybrid AI models	8	Understand CO1
Module 2: Power Estimation Techniques using AI Traditional power estimation methods, Machine Learning approaches for power estimation, Integration of AI models for accurate power prediction, Case studies on AI-driven power estimation	8	Apply CO2
Module 3: Hybrid AI Models for Power Optimization Combining AI techniques: Fuzzy Logic, Genetic Algorithms, Neural Networks, Designing hybrid models for power optimization, Simulation and analysis of hybrid models, Comparative study of hybrid vs. traditional models.	8	Analyse CO3
Module 4: Frameworks and Tools for AI-Driven VLSI Design Theoretical Foundations: Overview of AI model deployment in EDA workflows, Role of EDA tools in power modeling, synthesis, and simulation, Understanding how ML integrates into VLSI design stages (e.g., placement, routing, floor planning), Classification of AI tools: supervised vs. unsupervised in VLSI context. Introduction to tools: MATLAB/Simulink, Python-based platforms (TensorFlow, Scikit-learn, Keras) for AI model creation, EDA tools (Cadence Virtuoso, Synopsys Design Compiler) for VLSI design, Integration of AI models with design flow: input/output mapping, Tool interoperability challenges and solutions	8	Apply CO4
Module-5: Architectures in Hybrid AI-VLSI Systems Foundations of Hybrid AI Architectures: Overview of hybrid AI models: neuro-fuzzy, ANN-GA, RL-based architectures, Mapping AI algorithms to hardware: RTL-aware architecture planning, Trade-offs in accuracy, latency, power, and area for AI hardware integration. Low-Power Hardware Design Techniques for AI Systems: Power-aware logic synthesis and voltage scaling for AI cores, AI-based clock and power gating in logic blocks, Interconnect and memory hierarchy optimization for energy-efficient inference, Use of AI in VLSI architecture exploration and design-space optimization	8	Apply CO5

Yashappa

G

Additional Director & Principal
BNM Institute of Technology
Bangalore-560 076

Course Outcomes: After completing the course, the students will be able to	
25VDEP2151.1	Understand the integration of AI techniques in VLSI design for power efficiency.
25VDEP2151.2	Apply hybrid AI models to estimate and reduce power consumption in VLSI circuits.
25VDEP2151.3	Analyze the effectiveness of different AI methodologies in optimizing VLSI system performance.
25VDEP2151.4	Implement AI-driven VLSI designs utilizing contemporary tools and frameworks
25VDEP2151.5	Apply low-power design strategies for integrating hybrid AI models into VLSI systems, focusing on performance, energy efficiency, and hardware constraints.
25VDEP2151.6	Design and simulate VLSI systems incorporating hybrid AI models for enhanced power efficiency.

Reference Books
<ol style="list-style-type: none"> Saini, S., Lata, K., & Sinha, G. R. (Eds.). (2022). VLSI and hardware implementations using modern machine learning methods. CRC Press. Raj, B., Tripathi, S. L., Chaudhary, T., Rao, K. S., & Singh, M. (2024). Integrated devices for artificial intelligence and VLSI. Wiley-Scrivener. Iterative International Publishers. (2024). Advanced VLSI architectures: From concept to silicon. Iterative International Publishers. Janghel, S. R., & Sharma, S. C. (2020). <i>Hybrid intelligent systems: Analysis and design</i>. LAP Lambert Academic Publishing. Rabaey, J. M., Chandrakasan, A., & Nikolić, B. (2003). <i>Digital integrated circuits: A design perspective</i> (2nd ed.). Pearson Education.

Marks Distribution for Assessment:

PCC	CIA	SEA	CIA (50)			SEA Conduction: 100 M Reduced to: 50 M
				I	II	
Conduction	50	50	Written Test	50	50	Five questions with each of 20 marks (with internal choice). Student should answer one full question from each module
				Average of two tests – 25 Marks		
			Assignment	15		
			AAT	10		
			Total – 50 marks			

compilers to generate custom memory macros, Power/performance tuning using compiler options, Constraints-driven generation: area, access time, power. Refer Text Book 3.		
Module-5: Testing and Reliability in Low Power Memory		
RAM Fault design, Test algorithms for RAMs, Detection of Pattern sensitive Faults, BIST Architecture, BIST Techniques for RAM Chips, Test Generation and BIST for Embedded RAMs. Refer Text Book 4.	8	Evaluate CO5

Course Outcomes: After completing the course, the students will be able to	
25VDEP2152.1	Apply low power design principles to analyze power dissipation in CMOS circuits and memory cells, and evaluate different memory architectures for their suitability in low power applications.
25VDEP2152.2	Apply fault tolerance and redundancy techniques while analyzing noise, fault models, and radiation effects to enhance memory reliability and yield.
25VDEP2152.3	Apply knowledge of non-volatile memory cell operation to design flash memory arrays and evaluate their performance parameters including speed, endurance, and durability.
25VDEP2152.4	Apply architectural and circuit-level techniques to optimize memory power consumption, analyze trade-offs in memory banking and partitioning, and evaluate memory compiler options for power and performance optimization.
25VDEP2152.5	Apply RAM fault models and test algorithms to design BIST architectures and evaluate their test coverage and fault detection efficiency for embedded RAMs.

Reference Books	
1.	CMOS Memory Circuits, Tegze P. Haraszti, Kluwer Academic, E-Book Publisher: Springer, ISBN-13: 978-1475784107. Publication Date: March 21, 2013
2.	Flash Memories, Detlev Richter, Spinger, ISBN 978-94-007-6081-3, 2014
3.	Advanced Memory Optimization Techniques for Low-Power Embedded Systems, Manish Verma, Peter Marwedel, Publisher: Springer. ISBN-13 978-1-4020-5896-7, April 2013
4.	Digital Circuit Testing and Testability by Parag K Lala, Academic Press

Marks Distribution for Assessment:

PCC	CIA	SEA	CIA (50)			SEA Conduction: 100 M Reduced to: 50 M
				I	II	
Conduction	50	50	Written Test	50	50	Five questions with each of 20 marks (with internal choice). Student should answer one full question from each module
				Average of two tests – 25 Marks		
			Assignment	15		
			AAT	10		
				Total – 50 marks		

B.N.M. Institute of Technology

An Autonomous Institution under VTU
Dept. of Electronics and Communication Engineering
M. Tech (VLSI Design and Embedded Systems)

Semester: I

Course Name: Power semiconductor devices and Technology **Course Code: 25VDEP2153**

L: T: P: J	3: 0: 0 :0	CIE Marks: 50
Credits:	3	SEE Marks: 50
Hours/Week	3	SEE Duration: 03 Hours

Pre-Requisites: Embedded Systems and Sensors

Course Learning Objectives: The students will be able to

1	To provide a basic understanding of power device characteristics and their role in power electronics.
2	To build core understanding of semiconductor behavior and carrier dynamics for electronic device principles.
3	To understand the breakdown mechanisms and conduction limits in semiconductor devices for effective analysis and material selection in power applications.
4	To understand the structural features and key electrical behaviors of advanced rectifiers and transistor devices used in power electronics.
5	To understand the structure, operation, and performance factors of advanced SiC-based power devices for high-efficiency power applications.

Module-1: Introduction	No. of Hours	Blooms cognitive Levels
Ideal And Typical Power Device Characteristics, Unipolar Power Rectifiers, Bipolar Power Rectifiers, Unipolar Power Transistors, Bipolar Power Devices, MOS- Bipolar Power Devices	8	Understand CO1
Module-2: Material Properties		
Fundamental properties, energy band gap, intrinsic carrier concentration, junction built-in potential, zero bias depletion width, bulk electron mobility, bulk hole mobility, channel electron mobility, electron velocity field curve, hole velocity field curve	8	Understand CO2
Module-3: Breakdown Voltage		
Breakdown voltage: parallel plane breakdown, punch through breakdown, open base transistor breakdown, ideal specific on-resistance for one dimensional case, for silicon carbide, for gallium nitride	8	Understand CO3
Module-4: Schottky Rectifiers and P-i-N Rectifiers		
Schottky Rectifiers structure: Forward Conduction, Reverse Blocking, Shielded Schottky Rectifiers- Junction Barrier, P-i-N Rectifiers, structure, reverse blocking, reverse recovery, JFET Structure, SiC Planar power MOSFET structure.	8	Understand CO4
Module-5: Silicon Carbide Power devices		

By *emcyp/ks*

⑦

Additional Director & Principal
B.N.M. Institute of Technology
Bangalore

SiC BJT:structure and operation, breakdown voltage, current gain, SiC Gate turn off thyristors: structure and operation, forward blocking capability, switching characteristics, SiC IGBTs:n channel Asymmetric Structure, optimized n channel asymmetric structure, p-channel asymmetric structure.	8	Understand CO5
--	---	-------------------

Course Outcomes: After completing the course, the students will be able to	
25VDEP2153.1	Students will be able to describe key power device characteristics and their applications in power electronics systems.
25VDEP2153.2	Students will be able to explain semiconductor behavior and carrier dynamics essential to electronic device operation.
25VDEP2153.3	Students will be able to analyze breakdown mechanisms and conduction limits in semiconductor devices to guide material and device selection for power applications.
25VDEP2153.4	Students will be able to explain the structural design and electrical characteristics of advanced rectifiers and transistor devices in power electronics.
25VDEP2153.5	Students will be able to analyze the structure and operation of advanced SiC power devices and evaluate their performance characteristics for efficient power system design.

Reference Books
<ol style="list-style-type: none"> 1. B. J. Baliga, <i>Gallium Nitride and Silicon Carbide Power Devices</i>, World Scientific, 2017. 2. Hongyu Yu, Tianli Duan, <i>Gallium Nitride Power Devices</i>, Pan Stanford, 2017 3. Research articles and technical reports in the area of Power semiconductor device experimentation, modeling and Fabrication. 4. B. Jayant Baliga, <i>Fundamentals of Power Semiconductor Devices</i>, Springer, 2008 5. B. J. Baliga., <i>Silicon Carbide Power Devices</i>, World Scientific, 2006. 6. Baliga, B. Jayant, <i>Power Semiconductor Devices</i>, PWS Publishing Co., Boston, 1996.

B.N.M. Institute of Technology

An Autonomous Institution under VTU
 Dept. of Electronics and Communication Engineering
 M. Tech (VLSI Design and Embedded Systems)

Semester: I

Course Name: Computer Aided Design of VLSI Circuits **Code:25VDEP2154**

L: T: P: J	3 : 0 : 0: 0	CIA Marks: 50
Credits:	3	SEA Marks: 50
Hours/Week (Total)	40	SEA Duration: 03 Hours

Pre-Requisites: Understanding of digital electronics basic concepts of VLSI architecture, design flow, CMOS technology, and layout design, knowledge of data structures such as trees, graphs, stacks, and queues used in optimization and physical design algorithms, Basic proficiency in programming languages such as C/C++ or Python, exposure to any EDA/CAD tools like Cadence, Synopsys, or Mentor Graphics

Course Learning Objectives: The students will be able to

- | | |
|---|--|
| 1 | Understand the concept of digital systems, how they can be optimized for area, power and cost, why it is advantageous to use physical design tools. |
| 2 | Implement the concept of the physical design cycle and develop algorithms (tools) for each design cycle step and optimize the digital system at architectural level. |
| 3 | Synthesize a given system starting with problem requirements, identifying and designing the building blocks, and then integrating blocks designed earlier |
| 4 | Develop their own platform (tool) for specific application. |

Module-1	No. of Hours	Blooms cognitive Levels
-----------------	---------------------	--------------------------------

<p>High Level Synthesis: Hardware models - Internal representation - Allocation assignment and scheduling - Simple scheduling algorithm - Assignment problem - High level transformations.</p> <p>VLSI Simulation: Gate-level modelling and simulation - Switch-level modelling and simulation - Combinational Logic Synthesis - Binary Decision Diagram.</p>	8	Apply CO1
---	----------	------------------

<p>Module-2</p> <p>Data Structure and Basic Algorithms: Basic Terminology, Graph Search Algorithms Computational Geometry Algorithms.</p> <p>VLSI partitioning& floor planning: Problem Formulation, Classification of Partitioning Algorithms, Group migration Algorithms, Simulated Annealing and evolution algorithm, other partitioning algorithms. Problem formulation, classification, Constraint based, Integer programming based, rectangular dualization, simulated evolution floor planning algorithms.</p>	8	Apply CO2
--	----------	------------------

<p>Module-3</p> <p>Placement and Routing: Problem formulation, Classification, Simulation based, Partitioning based Placement Algorithms.</p> <p>Global Routing: Problem formulation, Classification, Maze routing Algorithms, Line Probe Algorithms, shortest path based Algorithms, Steiner tree based Algorithms Detailed Routing: Problem formulation, Classification single Layer routing, General river routing, Single row rotting.</p>	8	Apply CO3
---	----------	------------------

<p>Module-4</p> <p>Clock and Power Routing: Design considerations for the clocking system, delay calculation for clock trees, Problem formulation, Clock routing Algorithms, H-tree based Algorithms, MMM Algorithms, Geometric matching based Algorithms.</p> <p>Compaction: Classification of Compaction Algorithms, One-Dimensional & Two-Dimensional Compaction, Hierarchical Compaction</p>	8	Apply CO4
---	----------	------------------

S. Yashappa



Additional
 ENM Institute of Technology
 Bangalore-560 080

Module-5		
Genetic algorithm and its application in VLSI physical design: Terminologies – Simple Genetic algorithms, steady state algorithm – Genetic operators-types of GA-Genetic algorithms vs Conventional algorithms – GA example – GA for VLSI design. Genetic algorithm in partitioning, placement and routing.	8	Apply CO5

Course Outcomes: After completing the course, the students will be able to	
25VDEP2154.1	Analyse each stage of VLSI design flow.
25VDEP2154.2	Apply design knowledge to develop algorithms for VLSI design automation
25VDEP2154.3	Investigate the algorithms for optimizing VLSI design with respect to speed, power and area.
25VDEP2154.4	Design an optimized VLSI cell using various algorithms.
25VDEP2154.5	Utilize genetic algorithms to solve VLSI design problems such as partitioning, placement, and routing, and compare their effectiveness with traditional methods.

Reference Books	
1.	Pinaki mazumder and Elizabeth M Rudnick, "Genetic algorithms for VLSI design layout and test automation", Pearson Edition, 2011.
2.	N.A. Sherwani, "Algorithms for VLSI Physical Design Automation", Kluwar Academic Publishers, 2002, ISBN: 0-7923-8393-1
3.	S.H. Gerez, "Algorithms for VLSI Design Automation", John Wiley & Sons, 1998, ISBN: 978-0-471-98489-4

Marks Distribution for Assessment:

PBL	CIA	SEA	CIA (50)			SEA Conduction: 100 M Reduced to: 50 M		
			Theory	I IA	II IA	Five questions with each of 20 Marks (with internal choice). Student should answer one full question from each module		
Conduction	50	50	50	50	Average of 2 tests – 25 Marks			
			Assignment	15				
			AAT	10				
			Total – 50 Marks					Total – 50 Marks
			Total			50 Marks		

B.N.M. Institute of Technology

An Autonomous Institution under VTU
 Dept. of Electronics and Communication Engineering
 M. Tech (VLSI Design and Embedded Systems)

Semester: I

Course Name: RESEARCH METHODOLOGY AND IPR **Code: 25VDE216**

L: T :P: J: 0	3: 0 : 0 : 0	CIA Marks: 50
Credits	3	SEA Marks: 50
Hours/Week (Total)	3 (40)	SEA Duration: 03 Hours

Pre-Requisites: Use of internet and online database, clarity on research question/problem and basic of statistics

Course Learning Objectives: The students will be able to

1	To give an overview of the research methodology and explain the technique of defining a research problem
2	To explain the functions of literature review, carry out literature search and develop conceptual frameworks
3	To explain various experimental designs in research and data handling like data sampling and data collection methods
4	To interpret the research findings and prepare a research report
5	To build awareness on the various forms of IPR and manage a project and the related finances independently.

Module-1: Introduction to Research Methodology	No. of Hours	Blooms Cognitive Levels
<p>Research Methodology: Introduction, Meaning of Research, Objectives of Research, Motivation in Research, Types of Research, Research Approaches, Significance of Research, Research Methods versus Methodology, Research and Scientific Method, Importance of Knowing How Research is Done, Research Process, Criteria of Good Research</p> <p>Defining the Research Problem: Research Problem, Selecting the Problem, Necessity of Defining the Problem, Technique Involved in Defining a Problem, An Illustration Problems Encountered by Researchers in India.</p>	08	Apply CO1
<p>Module-2: Literature Review</p> <p>Reviewing the literature: Place of the literature review in research, bringing clarity and focus to your research problem, Improving research methodology, Broadening knowledge base in research area, enabling contextual findings, How to review the literature, searching the existing literature, reviewing the selected literature, developing a theoretical framework, Developing a conceptual framework, writing about the literature reviewed.</p> <p>Research Design: Meaning of Research Design, Need for Research Design, Features of a Good Design, Important Concepts Relating to Research Design, Different Research Designs, Basic Principles of Experimental Designs, Important Experimental Designs.</p>	08	Apply CO2
Module-3: Data Sampling and Testing of Hypothesis		

<p>Design of Sampling: Introduction, Sample Design, Sampling and Non-sampling Errors, Sample Survey versus Census Survey, Types of Sampling Designs. Measurement and Scaling: Qualitative and Quantitative Data, Classifications of Measurement Scales, Goodness of Measurement Scales, Sources of Error in Measurement Tools, Scaling, Scale Classification Bases, Scaling Technics, Multidimensional Scaling, Deciding the Scale. Data Collection: Experimental and Surveys, Collection of Primary Data, Collection of Secondary Data, Selection of Appropriate Method for Data Collection. Testing of Hypotheses: Hypothesis, Basic Concepts Concerning Testing of Hypotheses, Testing of Hypothesis, Test Statistics and Critical Region, Critical Value and Decision Rule.</p>	08	Apply CO3
Module-4: Interpretation and Report Writing		
<p>Interpretation: Meaning of Interpretation, Technique of Interpretation, Precaution in Interpretation. Report Writing: Significance of Report Writing, Different Steps in Writing Report, Layout of the Research Report, Types of Reports, Oral Presentation, Mechanics of Writing a Research Report, Precautions for Writing Research Reports.</p>	08	Analyze CO4
Module-5: Intellectual Property Rights and Project Management		
<p>Intellectual Property Rights: Intellectual Property: The Concept, Intellectual Property System in India, Development of TRIPS Complied, Regime in India, Various patent and deign acts of India. Project Management: Definition of project, characteristics of projects, types of projects, project roles. Strategic planning process, strategic objectives, identifying potential projects, feasibility study (environment, society), methods of selecting projects, prioritizing projects, securing and negotiating projects.</p>	08	Apply CO5

Course Outcomes: After completing the course, the students will be able to	
25VDE216.1	Apply understanding to formulate a clearly defined research problem.
25VDE216.2	Apply the theoretical knowledge of literature survey to carry out literature review for a paper publication
25VDE216.3	Implement appropriate sampling techniques and data collection methods in a research context.
25VDE216.4	Interpret the research findings and create a report
25VDE216.5	Apply principles of Intellectual Property Rights (IPR) and project management in real-world project scenarios.

Reference Books
1. C.R. Kothari, Gaurav Garg, "Research Methodology: Methods and Techniques", New Age International 4th Edition, 2018.
2. Ranjit Kumar, "Research Methodology a step-by-step guide for beginners" (For the topic Reviewing the literature under module 2), SAGE Publications 3rd Edition, 2011.
3. John J Hampton, Financial Management, PHI Publication, 4th edition, 2020 Trochim, "Research Methods: the concise knowledge base", Atomic Dog Publishing 2005.
4. Fink A, "Conducting Research Literature Reviews: From the Internet to Paper", Sage Publications 2009.
5. Timothy J Kloppenborg, Project Management, Cengage Learning, 2nd Edition, 2019.

PCC	CIA	SEA	CIA (50)			SEA
				I	II	Conduction: 100 M Reduced to: 50 M
Conduction	50	50	Written Test	50	50	Five questions with each of 20 marks (with internal choice). Student should answer one full question from each module
				Average of two tests – 25 Marks		
			Assignment	15		
			AAT	10		
			Total – 50 marks			

B.N.M. Institute of Technology

An Autonomous Institution under VTU
 Dept. of Electronics and Communication Engineering
 M. Tech (VLSI Design and Embedded Systems)

Semester: II

Course Name: VLSI Testing and Testability		Course Code: 25VDE221
L: T: P: J:	4: 0: 0: 0	CIE Marks: 50
Credits:	4	SEE Marks: 50
Hours	50	SEE Duration: 03 Hours
Pre-Requisites: Basic courses on Digital circuit design, Knowledge about simulation and Logic Design.		
Course Learning Objectives: The students will be able to		
1	Learn various types of faults and fault modelling	
2	Comprehend the need for testing and testable design of digital circuits	
3	Illustrate methods and algorithms for testing digital combinatorial networks and test pattern generation	
4	Exemplify methods for testing sequential circuits and memory testing	
5	Inferring testing methods using Boundary scan, Built-in self-test and other advanced topics in digital circuit design	
Module-1: Introduction, VLSI Testing Process and Fault Models		
	No. of Hours	Blooms Cognitive Levels
Testing Philosophy, Role of Testing, Digital and Analog VLSI Testing, VLSI Technology Trends affecting Testing, Types of Testing, Fault Modelling: Defects, Errors and Faults, Functional Versus Structural Testing, Levels of Fault Models, Single Stuck-at Fault. Text-1 1.1-1.4, 2.1.1, 4.1,4.2 and 4.5	10	Understand CO1
Module-2: Logic and Fault Simulation		
Simulation for Design Verification and Test Evaluation, Modelling Circuits for Simulation, Algorithms for True-value Simulation, Algorithms for Fault Simulation, ATPG. Fault Diagnosis of Digital Circuits, Test Generation Techniques for Combinational Circuits, Detection of Multiple Faults in Combinational Logic Circuits. Text-1 5.1 -5.5, Text - 3	10	Apply CO2
Module-3: Testability Measures		
SCOAP Controllability and Observability, High Level Testability Measures, Digital DFT and Scan Design: Ad- Hoc DFT Methods, Scan Design, Partial-Scan Design, Variations of Scan, Ad-Hoc DFT Methods. Text-1 6.1, 6.2, 14.1- 14.4	10	Apply CO3
Module-4: Built-In Self-Test		
The Economic Case for BIST, Random Logic BIST: Definitions, BIST Process, Pattern Generation, Response Compaction, Built-In Logic Block Observers, Test-Per-Clock, Test-Per Scan BIST Systems, Circular Self-Test Path System, Memory BIST, Delay Fault BIST, Logic Built in Self-Test. Text-1 15.1- 15.4	10	Apply CO4
Module-5: Boundary Scan Standard		
Motivation, System Configuration with BoundaryScan: TAP Controller and Port, Boundary Scan Test Instructions, Pin Constraints of the Standard, Boundary Scan Description Language: BDSLDescription Components, Pin Descriptions, Boundary Scan for Asynchronous Processor Text-1 16.1- 16.3	10	Apply CO5

Yeshajyothi

Additional Director
 BNM Institute of Technology
 Bangalore-560 070

Course Outcomes: After completing the course, the students will be able to	
25VDE221.1	Analyze the need for fault modeling and testing of digital circuits
25VDE221.2	Apply the concept of faults and failure models to generate the number of fault models for the given design under test (DUT)
25VDE221.3	Generate fault lists for digital circuits and compress the tests for efficiency
25VDE221.4	Design built-in self-tests for complex logic digital circuits
25VDE221.5	Apply boundary scan technique to validate the performance of digital circuits
25VDE221.6	Engage on Literature survey and make an effort to suggest new solution as a team

Reference Books	
1.	VLSI TESTING & DESIGN FOR TESTABILITY, Dr. A Chrispin Jiji, Dr. Y R Annie Bessant, Dr. J Grace Jency, Dr. S. Vanaja, Mrs. Iffat Fatima, Booksclinic Publishing, 2025
2.	Essentials of Electronic Testing for Digital, Memory and Mixed Signal VLSI Circuits -M.L.Bushnell, V. D. Agrawal, Kluwer Academic Publishers, 2002. Edition.
3.	Digital Systems and Testable Design - M. Abramovici, M.A.Breuer and A.D Friedman,Jaico Publishing House,2001
4.	Digital Circuits Testing and Testability - P.K. Lala, Academic Press,1997

Marks Distribution for Assessment:

PCC	CIA	SEA	CIA (50)			SEA Conduction: 100 M Reduced to: 50 M
				I	II	
Conduction	50	50	Written Test	50	50	Five questions with each of 20 marks (with internal choice). Student should answer one full question from each module
				Average of two tests – 25 Marks		
			Assignment	15		
			AAT	10		
			Total – 50 marks			Total – 50 marks

B.N.M. Institute of Technology

An Autonomous Institution under VTU
 Dept. of Electronics and Communication Engineering
 M. Tech (VLSI Design and Embedded Systems)

Semester: II

Course Name: Enhanced Techniques in Chip Design **Course Code: 25VDE222**

L: T: P: J	3: 0 :2: 0	CIA Marks: 50
Credits:	4	SEA Marks: 50
Hours/Week (Total)	5	SEA Duration: 03 Hours

Pre-Requisites: CMOS Logic Design, Power and energy relations in a capacitor, MOSFET Characteristics, Short channel effects in a MOSFET, Combinational and Sequential circuits.

Course Learning Objectives: The students will be able to

- 1 Understand the state-of-the-art approaches to power estimation and reduction.
- 2 Describe the various power reduction and the power estimation methods.
- 3 Explain power dissipation at all layers of design hierarchy from technology, circuit, logic, architecture and system.
- 4 Practice the low power techniques using current generation design style and process technology.
- 5 Understand the basics of High-Speed VLSI design methods.

Module-1: Introduction to Low power Design	No. of Hours	Blooms Cognitive Levels
<p>Introduction: Need for low power VLSI chips, charging and discharging capacitance, short circuit current in CMOS leakage current, static current, basic principles of low power design, low power figure of merits.</p> <p>Simulation power analysis: SPICE circuit simulation, discrete transistor modeling and analysis, gate level logic simulation, architecture level analysis, data correlation analysis in DSP systems, Monte Carlo simulation.</p>	10	Apply CO1
<p>Module-2: Power Estimation methods</p> <p>Probabilistic power analysis: Random logic signals, probability & frequency, probabilistic power analysis techniques, signal entropy.</p> <p>Circuit: Transistor and gate sizing, equivalent pin ordering, network restructuring and reorganization, special latches and flip flops, low power digital cell library, adjustable device threshold voltage.</p>	10	Apply CO2
<p>Module-3: Low power Design at Logic Level and Clock distribution</p> <p>Logic: Gate reorganization, signal gating, logic encoding, state machine encoding, pre-computation logic.</p> <p>Low power Clock Distribution: Power dissipation in clock distribution, single driver Vs distributed buffers, Zero skew Vs tolerable skew, chip & package co design of clock network.</p>	10	Apply CO3
<p>Module-4: Low power Design at Architecture/System Level</p> <p>Low power Architecture & Systems: Power & performance management, switching activity reduction, parallel architecture with voltage reduction, flow graph transformation.</p> <p>Low power arithmetic components: Introduction, circuit design style, adders, multipliers, division.</p>	10	Analyze CO4
<p>Module-5: Introduction to High-Speed VLSI Design</p> <p>Introduction to high-speed digital design: Frequency, time and distance issues in digital VLSI design. Capacitance and inductance effects, high speed properties of logic gates, speed and power. Modeling of wires,</p>	10	Apply CO5

Yashraj

3

Additional Director
 BNM Institute of Technology
 Bangalore

geometry and electrical properties of wires, Electrical models of wires, transmission lines, lossless LC transmission lines, lossy RLC transmission lines and special transmission lines.		
---	--	--

1. Design a traditional CMOS inverter schematic with 45 nm technology and plot its transfer (DC) characteristics and transient characteristics. Also, design a SC-SS (Low power) CMOS inverter schematic with 45 nm technology and plot its transfer (DC) characteristics and transient characteristics. Tabulate the readings (Delay, Power consumption, Power-Delay Product) for both the schematics and plot a comparison graph.
2. Design a traditional 2-input CMOS NAND gate schematic with 45 nm technology and plot its transfer (DC) characteristics and transient characteristics. Also, design a SC-SS (Low power) 2-input CMOS NAND gate schematic with 45 nm technology and plot its transfer (DC) characteristics and transient characteristics. Tabulate the readings (Delay, Power consumption, Power-Delay Product) for both the schematics and plot a comparison graph.
3. Design a traditional 2-input XOR gate (12T) schematics with 45 nm technology and plot its transfer (DC) characteristics and transient characteristics. Also, design a SC-SS (Low power) 2-input CMOS XOR gate schematic with 45 nm technology and plot its transfer (DC) characteristics and transient characteristics. Tabulate the readings (Delay, Power consumption, Power-Delay Product) for both the schematics and plot a comparison graph.
4. Design a traditional Half Adder schematic with 45 nm technology and plot its transient response. Also, design a SC-SS (Low power) Half Adder schematic with 45 nm technology and plot its transient response. Tabulate the readings (Delay, Power consumption, Power-Delay Product) for both the schematics and plot a comparison graph.
5. Design a traditional Full Adder schematic with 45 nm technology and plot its transient response. Also, design a SC-SS (Low power) Full Adder schematic with 45 nm technology and plot its transient response. Tabulate the readings (Delay, Power consumption, Power-Delay Product) for both the schematics and plot a comparison graph.
6. Design a traditional D Flip-Flop schematic with 45 nm technology and plot its transient response. Also, design a D Flip-Flop with self clock-gating schematic (Low power) with 45 nm technology and plot its transient response. Tabulate the readings (Delay, Power consumption, Power-Delay Product) for both the schematics and plot a comparison graph.
7. Design a 4-bit ripple carry adder schematic with 45 nm technology and plot its transient response. Also, design a 4-bit Carry save adder schematic with 45 nm technology and plot its transient response. Tabulate the readings (Delay, Power consumption, Power-Delay Product) for both the schematics and plot a comparison graph.
8. Design a basic 6T SRAM Cell schematic with 45 nm technology and plot its transient response. Also,

design a 10T SRAM Cell schematic with 45 nm technology and plot its transient response. Tabulate the readings (Delay, Power consumption) for both the schematics and plot a comparison graph.

EDA Tools: Cadence-Virtuoso, LT Spice.

Course Outcomes: After completing the course, the students will be able to

25VDE222.1	Identify the sources of power dissipation in CMOS circuits.
25VDE222.2	Perform power analysis using simulation-based approaches and probabilistic analysis.
25VDE222.3	Develop the optimization and trade-off techniques that involve power dissipation of digital circuits.
25VDE222.4	Apply the low power design techniques at the architecture and system level.
25VDE222.5	Apply and adopt the High-Speed VLSI techniques for various applications.
25VDE222.6	Develop the practical design techniques and their analysis at various levels of design abstraction and analyze how these are being captured in the latest design automation environments.

Reference Books

1. Practical Low Power Digital VLSI Design, Gary K. Yeap, Kluwer Academic Publishers, ISBN 978-1-4613-7778-8, 2012.
2. Low Power Design Methodologies, Jan M. Rabaey and Massoud Pedram, Kluwer Academic Publishers, 5th reprint, 2010.
3. Low-Power CMOS VLSI Circuit Design Kaushik Roy and Sharat Prasad, John Wiley, 2010.
4. Low-Power VLSI Circuits and Systems, Ajit Pal, Springer publications, 2015.

Marks Distribution for Assessment:

PCI	CIA	SEA	CIA (50)		SEA Conduction: 100 M Reduced to: 50 M
			I	II	
Conduction	50	50	Written Test	50	50
			Assignment	Average of two tests – 50 marks scaled down to 15 marks	
			Practical	Average of 2 Assignments – 10M	
				Weekly Assessment – 10 Marks IA test – 15 Marks (IA test to be conducted for 50 M and scaled down to 15M)	
			Total – 50 Marks	Total – 50 Marks	

Five questions with each of 20 marks (with internal choice). Student should answer one full question from each module

B.N.M. Institute of Technology

An Autonomous Institution under VTU
 Dept. of Electronics and Communication Engineering
 M. Tech (VLSI Design and Embedded Systems)

Semester: II

Course Name: Analog/Mixed mode signal IC design
Course Code: 25VDE223

L: T: P: J	3: 0: 2: 0	CIA Marks: 50
Credits:	4	SEA Marks: 50
Hours	50	SEA Duration: 03 Hours

Pre-Requisites: General considerations of MOS devices, MOS I/V Characteristics, second order effects, Basics to Amplifiers, Introduction to concepts of current mirrors and Op-Amp, Op-amp Parameters and Introduction to DAC and ADC.

Course Learning Objectives: The students will be able to

1	Describe the basic physics and operation of MOS devices
2	Exemplify single-stage and differential amplifiers and current mirrors
3	Describe operational amplifiers
4	Learn the design of phase-locked-loops
5	Know the role of Data converters in an ever-increasing digital world.

Module-1: Single stage Amplifier	No. of Hours	Blooms Cognitive Levels
Single stage Amplifier: Common Source stage, Source follower, Common-gate stage, Cascode Stage. Lab Experiment: 1 to 5	10	Understand CO1
Module-2: Differential Amplifiers		
Differential Amplifiers: Single ended and differential operation, Basic differential pair, Common mode response, Differential pair with MOS loads, Gilbert cell. Lab Experiment: 6 & 7	10	Apply CO2
Module-3: Passive and Active Current Mirrors & Operational Amplifiers (Part-1)		
Passive and Active Current Mirrors: Basic current mirrors, Cascode Current mirrors, Active Current mirrors. Operational Amplifiers (part-1): General Considerations, One Stage OP-Amp, Two Stage OP-Amp, Gain boosting Lab Experiment: 8	10	Apply CO3
Module-4: Operational Amplifiers (part-2) & Phase Locked Loops:		
Operational Amplifiers (part-2): Common Mode Feedback, Slew rate, Power Supply Rejection. Phase Locked Loops: Simple PLL, Charge pump PLLs, Non-ideal effects in PLLs, Delay-Locked Loops.	10	Apply CO4
Module-5: Data Converter Architectures:		
Data Converter Architectures: DAC & ADC Specifications, Current Steering DAC, Charge Scaling DAC, Cyclic DAC, Pipeline DAC. Flash ADC, Pipeline ADC, Integrating ADC	10	Understand CO5

Lab Experiments:

Additional Director & Principal
 BNM Institute of Technology
 Bangalore-560070

1. Design the Common Source amplifier with Current Source Load completing the design flow for

- a. Draw the schematic and verify the following
 - DC Analysis
 - AC Analysis
 - Transient Analysis

Yachappa

- b. Draw the Layout and verify the DRC, check for LVS, Extract RC and back annotate the same and verify the Design.
2. Design the Common Source **amplifier with Diode connected load** completing the design flow for
 - a. Draw the schematic and verify the following
 - DC Analysis
 - AC Analysis
 - Transient Analysis
 - b. Draw the Layout and verify the DRC, check for LVS, Extract RC and back annotate the same and verify the Design.
3. Design the Common Source **amplifier with resistive load** completing the design flow for
 - a. Draw the schematic and verify the following
 - DC Analysis
 - AC Analysis
 - Transient Analysis
 - b. Draw the Layout and verify the DRC, check for LVS d. Extract RC and back annotate the same and verify the Design.
4. Design the **Common Drain** with given specifications completing the design flow for
 - a. Draw the schematic and verify the following
 - DC Analysis
 - AC Analysis
 - Transient Analysis
 - b. Draw the Layout and verify the DRC, check for LVS d. Extract RC and back annotate the same and verify the Design.
5. Design the **Common Gate** with given specifications completing the design flow for
 - a. Draw the schematic and verify the following
 - DC Analysis
 - AC Analysis
 - Transient Analysis
 - b. Draw the Layout and verify the DRC, check for LVS, Extract RC and back annotate the same and verify the Design.
6. Design the **Current Mirror** with given specifications completing the design flow for
 - a. Draw the schematic and verify the following
 - DC Analysis
 - AC Analysis
 - Transient Analysis
 - b. Draw the Layout and verify the DRC. Check for LVS, Extract RC and back annotate the same and verify the Design.
7. Design the **Differential Amplifier** completing the design flow for
 - a. Draw the schematic and verify the following
 - DC Analysis
 - AC Analysis
 - Transient Analysis
 - b. Draw the Layout and verify the DRC. Check for LVS, Extract RC and back annotate the same and verify the Design.
8. Design an **op-amp** using the **differential amplifier** with Common source and Common Drain amplifier in library, completing the design flow mentioned below:
 - a. Draw the schematic and verify the following
 - DC Analysis
 - AC Analysis
 - Transient Analysis.
 - b. Draw the Layout and verify the DRC, Check for LVS, Extract RC and back annotate the same and verify the Design.

Course Outcomes: After completing the course, the students will be able to	
25VDE223.1	Derive small signal model of MOSFET with second order effects and estimate the parameters for single stage CS, CG, source follower and cascade stage.
25VDE223.2	Design high-performance, stable operational amplifiers with the tradeoffs between speed, precision and power dissipation, study the behaviour of phase-locked-loops for the applications.
25VDE223.3	Identify the critical parameters that affect the analog and mixed-signal VLSI circuits' performance.
25VDE223.4	Perform calculations in the digital or discrete time domain, more sophisticated data converters to translate the digital data to and from inherently analog world.
25VDE223.5	Apply concepts of both Analog and digital design for VLSI Technology.
25VDE223.6	Use efficient analytical tools for quantifying the behaviour of basic circuits by inspection.

Reference Books

1. Design of Analog CMOS Integrated Circuits Behzad Razavi TMH 2007
2. CMOS Circuit Design, Layout, and Simulation R. Jacob Baker Wiley Second Edition
3. CMOS Analog Circuit Design Phillip E. Allen, Douglas R. Holberg Oxford University Press Second Edition.

Marks Distribution for Assessment:

PCI	CIA	SEA	CIA (50)		SEA Conduction: 100 M Reduced to: 50 M	
			I	II		
Conduction	50	50	Written Test	50	50	Five questions with each of 20 marks (with internal choice). Student should answer one full question from each module
			Assignment	Average of two tests – 50 marks scaled down to 15 marks		
			Practical	Average of 2 Assignments – 10M		
				Weekly Assessment – 10 Marks IA test – 15 Marks (IA test to be conducted for 50 M and scaled down to 15M)		
				Total – 50 Marks	Total – 50 Marks	

Yashraj



Additional Director & Principal
BNM Institute of Technology
Bangalore-560 070

Dept. of Electronics and Communication Engineering
M.Tech (VLSI Design and Embedded Systems)
Choice Based Credit System (CBCS and Outcome Based Education (OBE))

Semester: II

Course Name: Advanced Functional Verification Methodologies

Course Code: 25VDE224

L: T: P: J	2: 0: 2: 2	CIA Marks: 50
Credits:	4	SEA Marks: 50
Hours/Week (Total)	6(50)	SEA Duration: 03 Hours

Pre-Requisites: Digital System Design, Testbench, Verilog HDL concepts and System Verilog Concepts

Course Learning Objectives: The students will be able to

- 1 Understand Verification Planning and Coverage-Driven Verification, UVM Testbench and environments
- 2 Understand and apply object-oriented programming (OOP) principles to design and implement UVM-based testbenches for functional verification.
- 3 Use key elements of the UVM library, including `uvm_object`, `uvm_component`, TLM, configuration, and factory mechanisms, to build organized verification testbenches.
- 4 Learn drivers, monitors, checkers, and test cases in a UVM testbench interact and contribute to functional coverage achievement.
- 5 Learn automation strategies to design and implement with agents, sequences, functional coverage, checkers, and reset handling.

Module-1: UVM overview:	No. of Hours	Blooms Cognitive Levels
UVM overview: Verification Planning and Coverage-Driven Verification, Multi-Language and Methodologies. UVM Testbench and environments, Interface UVCs, System and Module UVCs, the System Verilog UVM class library Lab : Demonstrate half adder using the UVM class library.	10	Apply CO1
Module-2: Advanced Object Oriented Programming Object Oriented Programming: Introduction, What is an object in OOP, Distributed development environment, Classes, Objects, Programs, Using generalization and inheritance, polymorphism in OOP, Downcast, Class libraries, Static methods and attributes, parameterized classes, packages and namespaces Lab : Demonstrate SystemVerilog Inheritance and polymorphism	10	Apply CO2
Module-3: UVM Library Basics UVM library basics: Using UVM library, Library Base Classes, the <code>uvm_object</code> class, the <code>uvm_component</code> class, UVM configuration mechanism, TLM in UVM, UVM factory, UVM message facilities, callbacks. Lab : Demonstrate program on UVM configuration mechanism	10	Apply CO3
Module-4: Interface UVCs Interface UVCs: Stimulus modeling and generation, creating the driver, creating the sequencer, connecting the driver and sequencer. Lab : Demonstrate for a 4-bit Adder how to create driver, sequencer, connecting the driver and sequencer.	10	Apply CO4
Module-5: Automating UVC Creation Automating UVC Creation: Creating the collector and monitor, modeling topology with UVM, creating the Agent, creating the UVM verification component, creating UVM sequences, configuring the sequencer's default sequence, coordinating end-of-test, implementing protocol-specific coverage and	10	Apply CO5

yashraj

Additional Director & Principal
BNM Institute of Technology
 Bangalore

checks, handling reset, packaging interface UVCs. Lab : Demonstrate TLM Concepts in UVM		
---	--	--

Projects:

1. Memory Controller Simulation
2. UVM-Based Verification of FIFO
3. UART Protocol Verification using UVM
4. SPI Master/Slave UVM Environment verification
5. AXI-Lite Interface Verification using UVM

Course Outcomes: After completing the course, the students will be able to	
25VDE224.1	Apply verification planning and functional coverage strategies to design and build UVM-based test benches.
25VDE224.2	Apply OOP principles to design and implement UVM test benches for functional verification.
25VDE224.3	Utilize UVM library elements (uvm_object, uvm_component, TLM interfaces, configuration objects, and the factory mechanism) to implement structured testbench architectures.
25VDE224.4	Analyze the interaction and contribution of UVM testbench elements driver, monitor, checker, and test cases in achieving functional coverage.
25VDE224.5	Implement automation strategies to develop reusable UVCs with agents, sequences, functional coverage, checkers, and reset handling.

Reference Books	
1.	Sharon Rosenberg, Kathleen Meade, “A Practical Guide to Adopting the Universal Verification Methodology (UVM)”, Lulu publishers, 2010.
2.	Vanessa R. Cooper, “Getting started with UVM: A beginner’s guide”, Verilab publisher, 2013.
3.	UVM Cookbook, Verification Academy, 2013.
4.	UVM User’s guide, Accellera, 2011.

Marks Distribution for Assessment:

PBL	CIA	SEA	CIA (50Marks)			SEA Conduction: 100 M Reduced to: 50 M
			Theory	I IA	II IA	Project Assessed for 100 marks reduced to 50 Marks
Conduction	50	50			25	
				Average of 2 tests – 25 marks		
			Practical	Weekly Assessment Lab Record/ Project-10 Marks Lab IA– 15 Marks		Total – 50 Marks
			Total – 50 Marks			

B.N.M. Institute of Technology

An Autonomous Institution under VTU
 Dept. of Electronics and Communication Engineering
 M. Tech (VLSI Design and Embedded Systems)

Semester: II

Course Name: Quantum-Driven VLSI Design **Course Code: 25VDEP2251**

L: T: P: J	3 :0 :0 :0	CIA Marks: 50
Credits:	3	SEA Marks: 50
Hours/Week (Total)	3	SEA Duration: 03 Hours

Pre-Requisites: Basic knowledge of VLSI design and digital electronics.

Course Learning Objectives: The students will be able to

- 1 Understand the fundamental principles of quantum mechanics and how they differ from classical digital systems.
- 2 Explore the architecture and behavior of quantum computing systems and logic gates.
- 3 Gain practical knowledge of designing and simulating quantum circuits using modern quantum design tools.
- 4 Analyze the integration challenges and methodologies of incorporating quantum devices into VLSI systems.
- 5 Investigate emerging trends and future technologies in quantum-driven VLSI and embedded system applications.

Module-1: Fundamentals of Quantum Mechanics for VLSI	No. of Hours	Blooms Cognitive Levels
Introduction to quantum mechanics: Qubits, superposition, entanglement. Quantum states and operators, Measurement in quantum systems, Comparison between classical bits and quantum bits, Implications of quantum mechanics on electronic devices.	8	Apply CO1
Module-2: Quantum Computing Principles Quantum logic gates: Pauli gates, Hadamard, CNOT, Toffoli, Quantum circuits and algorithms: Deutsch-Jozsa, Grover's algorithm, Quantum Fourier Transform and its applications, Error correction in quantum systems, Quantum teleportation and superdense coding.	8	Analyze CO2
Module-3: Quantum Devices and Integration with VLSI Quantum dots, single-electron transistors, and their characteristics, Integration challenges of quantum devices with CMOS technology, Design considerations for hybrid quantum-classical systems, Fabrication techniques for quantum devices	8	Analyze CO3
Module-4: Quantum VLSI Design Methodologies Design flow for quantum circuits, Simulation tools like Qiskit/ Cirq for quantum circuits, Power, area, and performance considerations in quantum VLSI, Case studies of quantum circuit implementations.	8	Analyze CO4
Module-5: Emerging Trends and Applications Quantum computing applications in cryptography, optimization, and machine learning, Quantum communication and networking, Future prospects of quantum technologies in VLSI, Ethical and societal implications of quantum computing.	8	Analyze CO5

Course Outcomes: After completing the course, the students will be able to

25VDEP2251.1	Comprehend quantum mechanical concepts such as superposition, entanglement, and measurement in the context of digital design.
--------------	---

Yashraj

G

Additional Director & Principal
 BNM Institute of Technology
 Bangalore - 560 070

25VDEP2251.2	Analyze quantum computing models and logic circuits relevant to VLSI
25VDEP2251.3	Design and simulate basic quantum circuits using modern tools like Qiskit or Cirq
25VDEP2251.4	Analyze the hardware integration challenges of quantum and classical VLSI systems
25VDEP2251.5	Analyze the impact of quantum devices and technologies on power, area, and timing trade-offs in VLSI design.
25VDEP2251.6	Apply quantum principles to solve real-time problems in domains such as cryptography, optimization, scheduling, and secure communication.

Reference Books

- Godwin Premi, M. S., Susitra, D., Mana, S. C., Velvizhi, R., & Nair, M. C. (2025). *Quantum computing*. Chennai: Magestic Technology Solutions Pvt. Ltd.
- Sahni, V. (2007). *Quantum computing with CD*. New Delhi: McGraw-Hill Education.
- Prasad, K. V. K. K., Shyamala, K., & Kogent Learning Solutions Inc. (2008). *VLSI design black book*. New Delhi: Dreamtech Press.
- Raj, B., Tripathi, S. L., Chaudhary, T., Rao, K. S., & Singh, M. (2024). *Integrated devices for artificial intelligence and VLSI: VLSI design, simulation and applications*. Boca Raton, FL: CRC Press.
- Raj, B. (2025). *Nanoelectronics: Materials to chips design*. Boca Raton, FL: CRC Press.
- Nielsen, M.A., & Chuang, I.L. (2010). *Quantum Computation and Quantum Information* (10th Anniversary Edition). Cambridge University Press.
- Weste, N.H.E., & Harris, D.M. (2010). *CMOS VLSI Design: A Circuits and Systems Perspective* (4th Edition). Pearson Education
- Sakurai, J.J., & Napolitano, J. (2020). *Modern Quantum Mechanics* (3rd Edition). Cambridge University Press.

Assessment processes:

PCC	CIA	SEA	CIA (50)			SEA Conduction: 100 M Reduced to: 50 M
				I	II	
Conduction	50	50	Written Test	50	50	Five questions with each of 20 marks (with internal choice). Student should answer one full question from each module
				Average of two tests – 25 Marks		
			Assignment	15		
			AAT	10		

B.N.M. Institute of Technology

An Autonomous Institution under VTU
 Dept. of Electronics and Communication Engineering
 M. Tech (VLSI Design and Embedded Systems)

Semester: II

Course Name: Scripting for EDA tool Automation **Course Code: 25VDEP2252**

L: T: P: J	3: 0 :0: 0	CIA Marks: 50
Credits:	3	SEA Marks: 50
Hours/Week (Total)	3	SEA Duration: 03 Hours

Pre-Requisites: Computer Basics, VLSI Basics.

Course Learning Objectives: The students will be able to

- 1 Understand the Basics of Linux commands
- 2 Explore the fundamentals of PERL Scripting concepts
- 3 Explain the advanced concepts of PERL Scripting language.
- 4 Present the TCL basics and advanced TCL scripting language.
- 5 Explore the fundamentals of Python and advanced Python concepts.

Module-1: Introduction to Linux	No. of Hours	Blooms Cognitive Levels
Introduction to Linux, File system of Linux, General usage of Linux Kernel and Basic Commands, Linux users and group, Permissions for file, directory and users, Searching a file and directory, Zipping and Unzipping concepts.	8	Understand CO1
Module-2: PERL Basics		
History and Concepts of PERL - Scalar Data - Arrays and List Data - Control structures – Hashes - Basics I/O - Regular Expressions – Functions - Miscellaneous control structures - Formats.	8	Apply CO2
Module-3: Advanced PERL Scripting		
Directory access - File and Directory manipulation - Process Management - Packages and Modules-Applications of PERL Scripts to Electronic Design Automation.	8	Apply CO3
Module-4: TCL Basics and Advanced TCL Scripting		
TCL Basics: An Overview of TCL and Tk -Tcl Language syntax – Variables – Expressions – Lists – Control flow – procedures - Errors and exceptions - String manipulations. Advanced TCL Scripting: Accessing files- Processes. Applications - Controlling Tools - Basics of Tk.	8	Apply CO4
Module-5: Python Basics and Advanced Python Scripting		
Introduction to Python-Using Python Interpreter-Brief tour on standard library-Control flow tools-Data Structures-Regular Expressions. Advanced Python Scripting: Input and output-Errors and Exceptions-Classes-Modules-Applications of Python scripts to Electronic Design Automation.	8	Apply CO5

Yashraj

2

Additional Director & Principal
 BNM Institute of Technology
 Bangalore-560070

Course Outcomes: After completing the course, the students will be able to	
25VDEP2252.1	Identify and apply various Linux commands to cater the needs of VLSI design.
25VDEP2252.2	Develop the PERL scripts for EDA tool automation.
25VDEP2252.3	Apply the various PERL scripts for handling files and directories.
25VDEP2252.4	Develop the TCL and advanced TCL scripts for VLSI design automation.
25VDEP2252.5	Develop the Python scripts to interpret files and directories.
25VDEP2252.6	Develop and execute various scripting methods for VLSI design applications.

Reference Books
<ol style="list-style-type: none"> 1. Larry Wall, Tom Christinsen, John Orwant, Programming PERL, Fourth Edition, Oreilly Publications, 2012. 2. Randal L. Schwartz, Brian D. Foy, Tom Pheonix, Learning PERL, 8th Edition, O'Reilly Media Inc, 2021. 3. John K. Ousterhout, Ken Jones, Tcl and TK Toolkit, Second Edition, Pearson Education, 2010. 4. Mark Lutz, Learning Python, 5th Edition, O'Reilly Media Inc, 2013. 5. Guido Van, Rossum Fred, L.Drake, Python Tutorial Release 3.2.2, Python Software Foundation, 2012.

Marks Distribution for Assessment:

PCC	CIA	SEA	CIA (50)		SEA Conduction: 100 M Reduced to: 50 M
			I	II	
Conduction	50	50		50	50
			Written Test	Average of two tests – 50 marks scaled to 25 marks	
			Assignment	15 marks	
			AAT	10 marks	
			Total – 50 Marks		Total – 50 Marks

B.N.M. Institute of Technology

An Autonomous Institution under VTU
Dept. of Electronics and Communication Engineering
M. Tech (VLSI Design and Embedded Systems)

Semester: II

Course Name: Embedded AI		Course Code: 25VDEP2253
L: T:P: J	3:0:0:0	CIA Marks: 50
Credits:	3	SEA Marks: 50
Hours	3	SEA Duration: 03 Hours

Pre-Requisites: Embedded Systems, RTOS, AI

Course Learning Objectives: The students will be able to

1	To Understand the fundamentals of Embedded Systems and Artificial Intelligence.
2	Explore how AI can be deployed on embedded hardware with resource constraints.
3	Apply machine learning techniques for real-time inference on microcontrollers.
4	Develop practical skills in deploying AI models on edge devices.

Module 1: Introduction to Embedded Systems and AI

Introduction to Embedded Systems and AI	No. of Hrs	Blooms cognitive Levels
Overview of Embedded Systems: Characteristics, applications, and constraints Basics of Artificial Intelligence and Machine Learning Embedded AI: Definition, relevance, and challenges	8	Understand CO1

Module 2: Microcontroller and Embedded Platform Fundamentals

Microcontroller and Embedded Platform Fundamentals	No. of Hrs	Blooms cognitive Levels
Architecture of ARM Cortex-M, RISC-V cores, Sensor interfacing and data acquisition, Real-time constraints and power optimization, Communication protocols: I2C, SPI, UART, BLE, RTOS overview for real-time AI applications	8	Understand CO2

Module 3: Machine Learning for Embedded Systems

Machine Learning for Embedded Systems	No. of Hrs	Blooms cognitive Levels
Model selection for embedded systems, Quantization, pruning, and compression techniques, Lightweight ML models: Decision trees, linear models, small CNNs, Overview of TinyML and TensorFlow Lite Micro, Data pipelines for embedded training/inference	8	Understand CO3

Module 4: Deployment Tools and Frameworks

Deployment Tools and Frameworks	No. of Hrs	Blooms cognitive Levels
TensorFlow Lite, Edge Impulse, CMSIS-NN, MicroTVM, Model conversion and deployment pipelines, Hands-on example: Training and deploying a model to detect gestures, Performance evaluation and metrics for edge AI	8	Apply CO4

Module 5: Applications and Case Studies

Yashraj

2

Additional Director & Principal
BNM Institute of Technology
Bangalore

Applications and Case Studies Smart health monitoring (e.g., fall detection, heart rate analysis), Predictive maintenance in IoT systems, Environmental monitoring using edge AI, Voice recognition and wake-word detection, Security, ethical concerns, and responsible AI in edge applications	8	Apply CO5
---	----------	--------------

Course Outcomes: After completing the course, the students will be able to	
25VDEP2253.1	Understand the architecture and constraints of embedded systems.
25VDEP2253.2	Explain AI concepts applicable to embedded platforms.
25VDEP2253.3	Apply lightweight machine learning models to real-world embedded problems.
25VDEP2253.4	Design and evaluate embedded AI applications using tools like TensorFlow Lite or Edge Impulse.
25VDEP2253.5	Integrate sensors, microcontrollers, and AI models for intelligent edge applications.
Reference Books	
<ol style="list-style-type: none"> 1. Pete Warden & Daniel Situnayake, <i>TinyML: Machine Learning with TensorFlow Lite on Arduino and Ultra-Low-Power Microcontrollers</i>, O'Reilly, 2019 2. Muhammad Ali Mazidi, <i>Embedded Systems Design using ARM Cortex-M Microcontrollers</i>, Wiley 3. David Patterson and John L. Hennessy, <i>Computer Organization and Design – RISC-V Edition</i>, Morgan Kaufmann 	

Assessment process

PCC	CIA	SEA	CIA (50)		SEA Conduction: 100 M Reduced to: 50 M	
			I	II		
Conduction	50	50	Written Test	50	50	
			Average of two tests – 25 Marks		Five questions with each of 20 marks (with internal choice). Student should answer one full question from each module	
			Assignment	15		
			AAT	10		
			Total – 50 marks	Total – 50 marks		

Design to Verification Mapping: Deriving test requirements from specs, Managing hierarchical verification SPICE Metric-Driven Verification: Verisium Manager flow for analog block verification AMS Verification Case Studies: Industry-relevant examples and metrics	8	Apply CO5
--	----------	------------------

Course Outcomes: After completing the course, the students will be able to	
25VDEP2254.1	Apply fundamental analog circuit concepts and model basic analog behavior using Verilog-A for verification purposes.
25VDEP2254.2	Apply Verilog-AMS to develop behavioral models for analog and mixed-signal components like ADCs and DACs.
25VDEP2254.3	Design and implement AMS testbenches using UVM-MS and simulate mixed-signal designs using tools like Spectre AMS Designer.
25VDEP2254.4	Apply randomization and assertion-based techniques to verify analog signal behavior and improve test coverage in mixed-signal verification.
25VDEP2254.5	Develop and manage a top-down AMS verification flow using real-number modeling and metric-driven approaches such as Verisium Manager.

Reference Books	
1.	Bramhananda Marathe, "Analog-Mixed Signal Verification", 1st Edition, 2015
2.	Janick Bergeron, Eduard Cerny, Alan Hunter, Andrew Nightingale, "Verification Methodology Manual for SystemVerilog", Springer, 1st Edition, 2005, ISBN: 0387255389
3.	"Verilog-AMS Language Reference Manual", Accellera Systems Initiative, 2014, Online link: <i>Accellera Verilog-AMS Downloads</i>
4.	Dennis Fitzpatrick, "Analog Design and Simulation Using OrCAD Capture and PSpice", 2nd Edition, Newnes, 2017, ISBN: 978-0081025055
5.	"Cadence Documentation on AMS Designer, Verisium, and UVM-MS", Cadence Design Systems
6.	IEEE Std 1800.2™-2020 – IEEE Standard for Universal Verification Methodology (UVM), https://ieeexplore.ieee.org/document/9099635

Marks Distribution for Assessment:

PCC	CIA	SEA	CIA (50)			SEA Conduction: 100 M Reduced to: 50 M	
			Theory	I IA	II IA	Five questions with each of 20 Marks (with internal choice). Student should answer one full question from each module	
Conduction	50	50			50		50
			Average of 2 tests – 25 Marks				
			Assignment	15			
			AAT	10			
			Total – 50 Marks			Total – 50 Marks	

i) CIA: 50%

Theory - 2 IA tests - Each of 50 Marks	Average of two tests scaled down to 25 Marks
Assignment: Two assignments- One for 10 marks and another for 5 marks	15 Marks
Additional Assessment Tools(AAT) : Oral/Online Quiz, Presentations, Group Discussions, Case studies, Term Paper, Open Ended Experiments, Mini industrial/ rural/ social projects, Two-minute video on latest topic, Short Mooc Courses, Practical Orientation on design thinking creativity and Innovation, Participatory & Industry Integrated learning, Practical activities, Problem solving exercises, Participation in Seminars/ academic events/ Symposia and any other activity.	10 Marks
Total	50 Marks

ii) SEA : 50%

Theory Exam	5 questions to answer each of 20 marks. 2 questions from each module with internal choice Students should answer one full question from each module	20 M X 5= 100 Marks Reduced to 50 Marks
Total		50 Marks

B.N.M. Institute of Technology

An Autonomous Institution under VTU
 Dept. of Electronics and Communication Engineering
 M. Tech (VLSI Design and Embedded Systems)

Semester: II

Course Name: AI-based control of Electrical Drives **Course Code: 25VDEP2255**

L: T: P: J **3: 0: 0 :0** **CIE Marks: 50**

Credits: **3** **SEE Marks: 50**

Hours/Week **3** **SEE Duration: 03 Hours**

Pre-Requisites: Embedded Systems and Sensors

Course Learning Objectives: The students will be able to

- | | |
|---|---|
| 1 | To understand the working principles and control techniques of special electrical machines used in various applications. |
| 2 | To learn about different advanced actuators and motors, like electromagnets, linear drives, and piezoelectric devices, and how they work. |
| 3 | To understand the construction, types, and working of magnetic bearings, mechanical power transmission elements, and support systems. |
| 4 | To learn how Artificial Intelligence is used in the control, analysis, monitoring, and industrial applications of electrical machines and drives. |
| 5 | To study the application of AI techniques in the analysis, control, monitoring, and performance optimization of induction machines, synchronous machines, reluctance motors |

Module-1: Motors For Continuous Rotation and Electromagnetic Stepping Drives	No. of Hours	Blooms cognitive Levels
Motors With Commutator, Brushless Permanent Magnet Motors, Switched Reluctance Motor, Rotating Field Motors, Classification of Stepping Motors, Control Of Stepping Motors, Operating Behavior of Stepping Motor.	8	Understand CO1

Module-2: Drives With Limited Motion and Piezo Electric Drives	No. of Hours	Blooms cognitive Levels
Electromagnets, Electrodynamic Linear and Multi Coordinate Drives, Linear and Planar Hybrid Stepping Motors, Physical Effect, Piezo Electric Components, Piezo Electric Actuators, Piezo Electric Motors, Driving Electronics	8	Understand CO2

Module-3: Magnetic Bearing Technology and Mechanical Transfer Units	No. of Hours	Blooms cognitive Levels
Passive Magnetic Bearings, Active Magnetic Bearing Systems, Gearings Couplings, Axles and Shafts, Bearings.	8	Understand CO3

Module-4: Application of Artificial Intelligence in Electric Drives- 1	No. of Hours	Blooms cognitive Levels
AI applications in electrical machines and drives including control, estimation, condition monitoring and diagnosis, industrial application of AI in drives. AI based steady state and transient analysis of d.c machines, estimators, control.	8	Understand CO4

Module-5: Application of Artificial Intelligence in Electric Drives- 2	No. of Hours	Blooms cognitive Levels
AI based steady state analysis and transient analysis of induction machines, AI based condition monitoring, diagnosis, parameter estimation, harmonic analysis, induction motor drive with real time fuzzy logic efficiency optimization controller, AI based steady state analysis and transient analysis of synchronous machines, AI based position estimation in switched reluctance motor drives.	8	Understand CO5

yash up the

5

Additional
B.N.M. Inst

Principal
of Technology

Course Outcomes: After completing the course, the students will be able to	
25VDEP2255.1	Students will be able to explain the operation and control of special electrical machines and apply this knowledge in practical electromechanical systems.
25VDEP2255.2	Students will be able to understand and explain the working and control of advanced motors and actuators used in precise motion and control systems.
25VDEP2255.3	Students will be able to identify and explain the function of magnetic bearings, gears, couplings, axles, shafts, and other mechanical components used in motion systems.
25VDEP2255.4	Students will be able to apply AI techniques for controlling, estimating, and diagnosing electrical machines and drives in both steady-state and dynamic conditions.
25VDEP2255.5	Students will be able to apply AI methods for steady-state and transient analysis, condition monitoring, fault diagnosis, and efficiency optimization in induction, synchronous, and switched reluctance motor drives.

Reference Books
<ol style="list-style-type: none"> 1. Hans Dieter Stoelting, <i>Handbook of fractional Horsepower Drives</i>, Springer, 1st edition, 2009 2. Ion Boldea, Syed A. Nasar, <i>Electric Drives</i>, CRC Press, 2nd Edition, 2005 3. Peter Vas, <i>Artificial Intelligence Based Electrical Machines and Drives: Application of Fuzzy, Neural and Genetic Algorithm Based Techniques</i>, Oxford University Press, 1999.

Marks Distribution for Assessment:

PCC	CIA	SEA	CIA (50)			SEA
				I	II	Conduction: 100 M Reduced to: 50 M
Conduction	50	50	Written Test	50	50	Five questions with each of 20 marks (with internal choice). Student should answer one full question from each module
				Average of two tests – 25 Marks		
			Assignment	15		
			AAT	10		
			Total – 50 marks			Total – 50 marks

Dept. of Electronics and Communication Engineering M.Tech (VLSI Design and Embedded Systems) Choice Based Credit System (CBCS and Outcome Based Education (OBE))		
Semester: II		
Course Name: Neuromorphic Chip Design and Computing		Course Code: 25VDE226
L: T: P: J	3: 0 :0: 0	CIA Marks: 50
Credits:	3	SEA Marks: 50
Hours/Week (Total)	3	SEA Duration: 03 Hours
Pre-Requisites: Basic knowledge of Artificial Neural Networks, FPGA, Analog circuits, Digital circuits.		
Course Learning Objectives: The students will be able to		
1	Understand the current trends and methods in Neuromorphic Computing.	
2	Explore the basics of biological neural circuits.	
3	Present the Neuromorphic computing systems.	
4	Discuss the fundamentals of neuromorphic devices, circuits and systems.	
5	Understand the design of Hardware Accelerators using DNNs.	
Module-1: Introduction to Neuromorphic Computing		
	No. of Hours	Blooms Cognitive Levels
Brain as a potential Technology: The nature of Neuronal Computation, approaches to understanding Brains, an example model of Neural circuit processing, Toward Neuromorphic cognition. Artificial Neural Networks in Hardware: Digital Accelerators, FPGA-Based Accelerators, Analog/Mixed-Signal Accelerators.	8	Understand CO1
Module-2: Hardware implementation of Spiking Neural Networks		
Different generations of Neural Networks, Spiking Neuron operating principle, Models of spiking Neurons, Methods of Data Representation in Spiking Neural Networks and Network Learning Methods, Assessment of Network Processing Efficiency, Edge computing using Spiking Neurons, Hardware aspects of Semiconductor implementations of Spiking Neurons, Neuro-processors.	8	Apply CO2
Module-3: Building Neuromorphic Systems-Silicon Neurons		
Introduction, Silicon Neuron Circuit Blocks, Conductance Dynamics Spike-Event Generation, Spiking thresholds and Refractory periods, Spike-Frequency adaptation and adaptive thresholds, Axons and Dendritic trees, Additional useful building blocks, Silicon Neuron implementations, Subthreshold biophysically realistic models, Compact I & F circuits for Event-based systems, Generalized I & F Neuron circuits, Above threshold, Accelerated-Time, and Switched-Capacitor Designs.	8	Apply CO3
Module-4: Building Neuromorphic Systems- Silicon Synapse		
Introduction, Silicon synapse implementations, non-conductance-based circuits, Conductance-based circuits, NMDA synapse, Dynamic plastic synapses, Short-Term plasticity, Long-Term plasticity.	8	Apply CO4
Module-5: Accelerating DNNs in Hardware		
GPUs, Spatial Accelerators, Systolic Arrays, HW-SW co-design, Binary neural networks, Bit-precision, pruning and sparsity, vector architectures, FPGAs and GPU Architectures, ASIC Accelerators, In-Memory computing accelerator design, Neuromorphic accelerators, custom and reconfigurable accelerators, Emerging technologies, ReRAM, Analog Accelerators, Emerging Hardware Architectures, Memristor based designs, Spiking architectures.	8	Apply CO5

Yashraj
11/6/26

Course Outcomes: After completing the course, the students will be able to	
25VDE226.1	Understand the various aspects of computational neuroscience.
25VDE226.2	Design the hardware-based Neural Networks.
25VDE226.3	Develop the neuromorphic computing systems for various applications.
25VDE226.4	Model the neuromorphic blocks using devices, circuits and systems.
25VDE226.5	Design neuromorphic accelerators using DNNs for various applications.
25VDE226.6	Develop the VLSI design applications using neuromorphic computing technologies.

Reference Books
1. Abderazek Ben Abdallah and Kang Dang Ngo, Neuromorphic Computing Principles and Organization, First Edition, Springer, 2022.
2. Liu Shih-Chi, Tobi Delbruck, Giacomo Indiveri, Adrain Whatley, and Rodney Douglas, Event-Based neuromorphic systems, John Wiley & Sons, 2014.
3. Gerstner, Wulfram, Werner M. Kistler, Richard Naud and Liam Paninski, Neuronal dynamics: From Single Neurons to Networks and Models of Cognition, Cambridge University press, 2014.

Marks Distribution for Assessment:

PCI	CIA	SEE	CIA (50)		SEE Conduction: 100 M Reduced to: 50 M	
			I	II		
Conduction	50	50	Written Test	50	50	
			Average of two tests - 25 marks		Five questions with each of 20 marks (with internal choice). Student should answer one full question from each module	
			Assignment	15M		
			AAT	10M		
Total – 50 Marks					Total – 50 Marks	