B. N. M Institute of Technology

An autonomous Institution under VTU

IEEE Circuits and System Society (SBC 14831A)

List of Events Organized in 2026

Sl. No.	Event Title	Date	No. of Participants
1	Design Verification using System Verilog	13th July 2026 to 31st July 2026	67
2	Outreach Program	25th July 2026	30
3	Boot Camp on Open-Source SoC Design and Verification using Verilator and Yosys	29th June 2026 to 3rd July 2026	82
4	Field/Exposure Visit to ISRO U R Rao Satellite Centre (URSC), Bengaluru	19th June 2026	126
5	Diffuse the Bomb	30th May 2026	75
6	Alumni Series Talk on Ethical Issues on Vision AI	17th April 2026	120
7	Avinya 2026 – Project Exhibition	11th April 2026	120

8	Robo Track	26th March 2026	71
9	Robo Knockout	25th March 2026	30
10	Industrial Visit to IISc on OPEN DAY 2026	7th March 2026	30
11	Rig to Solder	18th February 2026	60
12	Future of Automotive: How E/E Architecture is Powering the Shift to Software-Defined Vehicles	14th February 2026	66
13	Road Map to IITs and PSU Jobs through GATE	8th January 2026	62
14	Awareness Workshop on Semiconductor Technologies	19th December 2025	53
15	Circuit Theatre – IEEE Week 2025	16th October, 2025	60
16	NXP Campus Connect Webinar on “SRAM and ROM IP Architecture and Design	02nd September, 2025	50
17	Internship on Design, Modeling, and Simulation of Digital Circuits using Verilog	21st July, 2025 to 09th August 2025	64
18	Industrial Visit to BMRCL	12th July 2025	135

19	Industrial Visit to DSedify	4th July, 2025	50
20	Technical Talk on VLSI Industry Prospects: Core Opportunities for ECE Graduates	27th June 2025	100
21	Masterclass on Higher Education (Abroad Studies)	26th June 2025	42
22	Internship on Design Verification using System Verilog	02nd June 2025 to 20th June 2025	64
23	Avinya 2025 – Project Exhibiton	12th May 2025	120

IEEE CAS BNMIT Office Bearers

Sl. No	Name	Position Held
1	Debarati Mukherjee	Chair
2	Manish L, Harshini H L	Vice-Chair
3	Shreyas S, Manjushree S	Secretary
4	Dhruv M N	Treasurer
5	Akanksha Sharma, Amogh M S	Webmaster

Faculty Advisor : Dr. Yasha Jyothi M Shirur

BNM Institute of Technology

An autonomous Institution under VTU

Title of the Event: “Internship on Design Verification Using System Verilog”

Date: 13th July to 31st July, 2026 Time: 9:00 AM to 4:00 PM

Venue: N502, B.N.M. Institute of Technology, Bengaluru

Participants: 67

Semester/Section: 5th Semester UG ECE Students

Organized by:

Department of Electronics and Communication Engineering

B.N.M. Institute of Technology, Bengaluru

In Association with:

IEEE Circuits and Systems Society (IEEE CASS)

IEEE Geoscience and Remote Sensing Society (IEEE GRSS)

Cranes Varsity Pvt. Ltd., Bengaluru

Faculty Coordinators:

Dr. Subodh Kumar Panda

Dr. Smitha Gayathri D

Resource Person:

Ms. Kanchana H., Trainer and Subject Matter Expert, Cranes Varsity Pvt. Ltd.

Overview :

A 15-Day Internship on “Design Verification Using System Verilog” was organized by the Department of Electronics and Communication Engineering, B.N.M. Institute of Technology, Bengaluru, in association with Cranes Varsity Pvt. Ltd., Bengaluru. The internship was

conducted from 13th July 2026 to 31st July 2026 and was aimed at providing 5th semester UG ECE students with industry-relevant knowledge and practical skills in VLSI design, RTL development and functional verification using System Verilog.

The programme combined technical lectures with extensive hands-on laboratory sessions, assignments, quizzes, project development and evaluation. The internship provided students with practical exposure to modern RTL design methodologies, SystemVerilog-based verification techniques and industry-oriented verification practices used in semiconductor development.

A total of 67 students from the Department of Electronics and Communication Engineering actively participated in the internship. Throughout the programme, students attended technical sessions, completed assignments, participated in quizzes, developed individual verification projects and presented their work during the final project evaluation.

The internship was conducted with the support of Cranes Varsity Pvt. Ltd., which provided industry-oriented training in VLSI Design and SystemVerilog Verification. Ms. Kanchana H., Trainer and Subject Matter Expert, conducted technical sessions, hands-on laboratory training and project mentoring, providing students with valuable industry exposure.

Topics Covered :

The internship curriculum provided a systematic understanding of RTL design and functional verification. The major topics covered during the programme included:

- Introduction to VLSI Design Flow
- Semiconductor Fundamentals
- CMOS Technology Basics
- Verilog HDL Fundamentals
- RTL Coding Techniques
- Combinational and Sequential Circuit Design
- Finite State Machine Design
- AXI4 Protocol Fundamentals
- AXI4 Read and Write Transactions

- Introduction to SystemVerilog
- SystemVerilog Data Types and Procedural Blocks
- Interfaces and Arrays
- Object-Oriented Programming Concepts
- Constrained Random Verification
- Assertions and Functional Coverage
- Layered Testbench Architecture
- Driver, Monitor, Generator and Scoreboard
- Transaction-Level Communication
- Introduction to Universal Verification Methodology (UVM)
- Project Development and Verification Methodology

Software and Tools Used :

Students gained practical experience using the following software platforms and development tools:

- EDA Playground
- Xilinx Vivado
- GitHub for project version control and code sharing

These tools were used for RTL development, simulation, waveform analysis, functional debugging and validation of digital designs.

Event Proceedings :

1. The programme began with an introduction to semiconductor fundamentals, CMOS technology and the complete VLSI design flow. Students gained an understanding of the different stages involved in developing modern digital integrated circuits.

2. Students were introduced to Verilog HDL and RTL coding techniques, followed by practical implementation of combinational and sequential circuits. The sessions helped students understand how hardware functionality can be represented using RTL.

3. The programme covered Finite State Machine (FSM) design, enabling students to understand state-based digital systems and their implementation using RTL methodologies.

4. Students received detailed exposure to the AXI4 protocol, including AXI4 architecture, read and write transactions and protocol communication mechanisms. This provided an understanding of commonly used on-chip communication protocols.

5. The internship then progressed to SystemVerilog, covering SystemVerilog data types, procedural blocks, interfaces and arrays. Students learned how SystemVerilog extends Verilog to support advanced verification methodologies.

6. Object-Oriented Programming concepts such as classes, objects and related SystemVerilog features were introduced to help students understand the development of reusable verification components.

7. Students were trained in constrained random verification, enabling them to generate varied test scenarios and improve verification effectiveness.

8. The programme covered assertions and functional coverage, providing students with techniques for automatically checking design behaviour and measuring verification completeness.

9. Students learned about layered testbench architecture and the roles of the Generator, Driver, Monitor and Scoreboard. These concepts helped them understand how reusable and self-checking verification environments are constructed.

10. The internship introduced Transaction-Level Communication and provided an overview of the Universal Verification Methodology (UVM), exposing students to structured and industryoriented verification methodologies.

11. Throughout the internship, students participated in hands-on laboratory exercises involving

RTL implementation, simulation, waveform analysis and debugging. They used EDA Playground and Xilinx Vivado to develop and verify their designs.

12. As part of the project component, each student developed an individual project involving RTL design and SystemVerilog-based functional verification. The project activities included requirement analysis, RTL implementation, self-checking testbench development, constrained random verification, assertion-based checking, functional coverage, debugging, simulation and documentation.

13. Students maintained their project work using GitHub, gaining practical experience in version control and code sharing. The projects covered application areas such as communication protocols, memory subsystems, digital controllers, arithmetic units, bus interfaces and verification environments.

14. A one-day Hackathon was conducted on the final day of the internship. Students were given time-bound technical problem statements requiring design implementation, verification planning, debugging, simulation and presentation. The Hackathon encouraged innovation, analytical thinking, teamwork and rapid problem-solving.

15. The internship concluded with project demonstrations, evaluations, assessments and feedback activities. Students presented their technical work and demonstrated the verification methodologies they had learned during the programme. The report also documents project demonstrations and the online test conducted by Cranes Varsity.

Objective :

The major objectives of the internship were to:

- Introduce students to the complete VLSI design and verification flow.
- Develop a strong foundation in Verilog HDL and RTL design.
- Familiarize students with SystemVerilog and modern verification methodologies.
- Understand AXI4 protocol fundamentals and protocol verification.
- Develop reusable and self-checking testbenches.
- Apply constrained random verification techniques.
- Understand assertions and functional coverage.

- Introduce layered testbench architecture and UVM concepts.
- Enhance simulation, debugging and waveform-analysis skills.
- Provide hands-on exposure to industry-oriented EDA tools.
- Develop project development, documentation and presentation skills.
- Improve teamwork, analytical thinking and problem-solving abilities.

Conclusion :

The 15-Day Internship on “Design Verification Using System Verilog” successfully provided students with a comprehensive learning experience in VLSI design and functional verification. The combination of theoretical sessions, practical laboratory exercises, project development, assessments and the final Hackathon enabled students to apply their knowledge to real-worldoriented digital design and verification problems.

Photograph :


Lenovo
Lenovo

BNM Institute of Technology

An autonomous Institution under VTU

Title of the Event: “Outreach Program”

Date: 25th July, 2026 Time: 9:00 AM to 1:00 PM

Venue: Sri Jayabharathi School Participants: 30

Semester/Section: 5th & 7th Semesters

Organized by:

IEEE CASS

IEEE RAS

IEEE CS

IEEE PES

IEEE SPS

IEEE WIE

IEEE EMBS

IEEE GRSS

IEEE COMSOC

B.N.M. Institute of Technology (Autonomous), Bengaluru

Staff Coordinators:

Mr. Kiran K N

Dr. Priyashree S

Overview:

An outreach program was organized by IEEE BNMIT at Sri Jayabharathi School, with active participation from students of the 5th and 7th semesters. The program aimed to bridge the gap between school education and engineering by introducing school students to various technological domains through live demonstrations and interactive sessions. Undergraduate

students showcased their innovative projects and explained their fundamental concepts, working principles and realworld applications.

Event Proceedings:

1. The outreach program was organized to create awareness among school students about emerging technologies and their applications in solving real-world problems. The initiative provided students with an opportunity to experience engineering beyond textbooks and encouraged them to develop an interest in science, technology and innovation.

2. Students from the 5th and 7th semesters demonstrated a variety of engineering projects to school students and faculty members. The projects represented multiple technological domains, including Robotics, Embedded Systems, Signal Processing, Internet of Things (IoT), and Electronics.

3. Each project team explained the objectives, design, implementation, hardware components and software involved in their respective projects. The students also demonstrated the functionality of their projects in real time, allowing the school students to gain practical exposure to engineering applications.

4. The school students actively participated in the sessions by asking questions, interacting with the project models and learning about different engineering disciplines. The interactive demonstrations created an engaging learning environment and encouraged curiosity, creativity and scientific thinking among the participants.

5. The outreach initiative also provided valuable learning opportunities for the undergraduate students. By explaining complex engineering concepts to a younger audience in a simple and understandable manner, the students improved their technical presentation, communication and interpersonal skills.

6. The undergraduate participants also gained confidence in public speaking, teamwork and project demonstration while interacting with a diverse audience. The activity provided them with an opportunity to share their technical knowledge and strengthen their communication and leadership abilities.

7. The school students gained a better understanding of modern technologies such as robotics, embedded systems and signal processing through practical demonstrations. The exposure helped them understand engineering applications and encouraged them to explore science, technology, engineering and mathematics (STEM).

8. Overall, the outreach program promoted knowledge sharing between institutions and encouraged innovation through hands-on learning experiences. The interaction between undergraduate students and school students created a meaningful platform for exchanging knowledge and inspiring young learners towards technology and engineering.

Objective:

- The primary objectives of the outreach program were to:
- Create awareness among school students about emerging technologies and their real-world applications.
- Introduce students to practical projects from different engineering domains.
- Inspire young students to pursue higher education in engineering and technology.
- Enhance the communication, presentation and teamwork skills of undergraduate students.
- Encourage knowledge sharing between undergraduate students and school students.
- Promote innovation, curiosity and scientific thinking through hands-on demonstrations.
- Motivate school students to explore careers in Science, Technology, Engineering and Mathematics (STEM).

Conclusion:

The Outreach Program at Sri Jayabharathi School was successfully conducted and effectively promoted technical awareness and experiential learning among school students. The live demonstrations covering Robotics, Embedded Systems, Signal Processing, IoT and Electronics generated enthusiasm and curiosity while providing valuable insights into modern engineering practices. The interaction also enabled undergraduate students to strengthen their communication, presentation and leadership skills by sharing their knowledge with younger learners. Overall, the program successfully achieved its objective of fostering technological awareness, encouraging innovation and inspiring the next generation of engineers through meaningful interaction and hands-on project demonstrations.

Event Images :

Figure 1: Group photograph of undergraduate students, school students, faculty members and organizers during the outreach program at Sri Jayabharathi School.

BNM Institute of Technology

An autonomous Institution under VTU

Title of the Event: “Boot Camp on Open-Source SoC Design and Verification using Verilator and Yosys”

Date: 29th June to 3rd July, 2026 Time: 10:00 AM to 4:00 PM

Venue: B.N.M. Institute of Technology, Bengaluru

Participants: 82

Semester/Section: 7th Semester ECE Students & 2nd Year M.Tech Students

Organized by:

IEEE Circuits and Systems Society (IEEE CASS)

Department of Electronics & Communication Engineering B.N.M. Institute of Technology (Autonomous), Bengaluru

In Collaboration with:

National Institute of Electronics and Information Technology (NIELIT), Calicut

Staff Coordinators:

Dr. Yasha Jyothi M Shirur, HoD, Dept. of ECE

Dr. Smitha Gayathri D, Associate Professor, ECE

Dr. Manjunath G Astuti, Associate Professor, ECE Dr. Priyadarshini K Desai, Associate Professor, ECE

Overview :

The Department of Electronics and Communication Engineering, BNMIT, in collaboration with the National Institute of Electronics and Information Technology (NIELIT), Calicut, organized a five-day Boot Camp on Open-Source SoC Design and Verification using Verilator and Yosys from 29th June to 3rd July 2026. Conducted under the guidance of experts from NIELIT, the program was designed to provide students with practical exposure to industrystandard methodologies used in modern System-on-Chip (SoC) design and verification.

Event Proceedings :

1. The five-day boot camp was organized with the objective of bridging the gap between theoretical knowledge acquired in classrooms and real-world VLSI design practices. Through intensive hands-on sessions, participants gained practical experience with open-source Electronic Design Automation (EDA) tools and developed an understanding of the RTL design, verification, synthesis and IP integration workflow.

2. The boot camp introduced participants to the complete open-source digital design ecosystem used in semiconductor industries. The training focused on practical skills in RTL simulation, logic verification, synthesis and subsystem integration using widely adopted open-source tools.

3. The training followed a progressive learning approach, beginning with Linux fundamentals and gradually advancing towards complete SoC-level design integration. Participants learned how digital hardware progresses from Register Transfer Level (RTL) descriptions to synthesized gatelevel implementations while gaining exposure to debugging, verification and design optimization practices.

4. The first day focused on the Linux environment and Vi Editor. Participants learned essential terminal commands, directory navigation, file management, permissions, shell utilities and scripting basics. The Vi editor was also introduced to enable efficient source-code editing within Linux-based VLSI development environments.

5. The second and third days focused on RTL Design and Functional Verification using Verilator. Participants designed and verified combinational and sequential digital circuits while learning verification methodologies, waveform generation and debugging techniques. Laboratory exercises included logic gates, multiplexers, half adder, full adder, JK flip-flop, 4-bit counter and ripple counter.

6. Participants also gained exposure to GTKWave for waveform visualization, enabling them to perform detailed timing analysis and functional verification of RTL designs. This helped participants understand how simulation waveforms can be used to identify and debug design issues.

7. The fourth day introduced RTL Synthesis using Yosys. Participants learned how RTL descriptions are converted into optimized gate-level netlists through different synthesis stages, including process conversion, optimization passes, technology mapping and logic optimization.

8. Students also explored synthesis targeting the SkyWater 130 nm Process Design Kit (PDK). This provided valuable insight into how RTL designs are mapped onto actual semiconductor technology libraries and helped participants understand the connection between digital design and semiconductor implementation.

9. The fifth day focused on System-on-Chip integration and low-power design. Participants learned how multiple Intellectual Property (IP) blocks can be interconnected to build complete digital systems. Practical exercises included a UART Receiver, APB Bus Interface and APBUART Bridge.

10. The modules were integrated into a mini SoC project, through which participants explored clock-domain synchronization, reset management, debugging methodologies and introductory low-power design techniques commonly used in industrial SoC development.

11. Throughout the boot camp, participants gained practical experience with several open-source EDA tools and technologies, including the Linux Operating System, Vi Editor, Verilator, GTKWave, Yosys Open Synthesis Suite and SkyWater 130 nm PDK.

12. The hands-on nature of the training enabled participants to develop and verify digital circuits, build RTL simulation environments, perform synthesis and technology mapping, analyze simulation waveforms, and understand subsystem-level IP integration within SoC architectures.

13. The boot camp also provided participants with a strong foundation for advanced VLSI topics such as Clock Domain Crossing (CDC), Reset Domain Crossing (RDC), Design for Testability (DFT) and low-power verification.

Objective :

The primary objectives of the boot camp were to:

- Bridge the gap between theoretical VLSI knowledge and practical semiconductor design practices.

1. Provide hands-on experience with open-source EDA tools used in RTL design and verification.
2. Develop practical skills in RTL simulation, functional verification and debugging.
3. Introduce participants to RTL synthesis and technology mapping using Yosys.
4. Provide exposure to the SkyWater 130 nm Process Design Kit and open-source semiconductor technology libraries.
5. Develop an understanding of IP integration and System-on-Chip architectures.
6. Introduce participants to clock synchronization, reset management and low-power design concepts.
7. Build a strong foundation for advanced VLSI design and semiconductor engineering applications.

Conclusion :

The five-day Boot Camp on Open-Source SoC Design and Verification was an enriching learning experience for the participants. By combining theoretical concepts with extensive laboratory exercises, the program successfully introduced students to the complete RTL-to-gatelevel design flow followed in modern semiconductor industries. The hands-on exposure to Linux, Verilator, GTKWave, Yosys and the SkyWater 130 nm PDK enabled participants to understand practical aspects of digital IC design beyond the conventional classroom curriculum. The boot camp significantly strengthened participants' knowledge in RTL design, verification methodologies, synthesis and SoC integration while preparing them for future careers in VLSI design and semiconductor engineering.

The Department of Electronics and Communication Engineering extends its sincere appreciation to the experts from NIELIT Calicut for conducting the informative and industry-relevant training program, and to all faculty coordinators and participants for contributing to its successful execution

Event Images :

Figure 1: Group photograph of participants, faculty coordinators and NIELIT experts at the completion of the five-day Boot Camp.

BNM Institute of Technology

An autonomous Institution under VTU

Title of the Event: “Field/Exposure Visit to ISRO U R Rao Satellite Centre (URSC), Bengaluru”

Date: 19th June, 2026

Time: 8:30 AM

Venue: ISRO U R Rao Satellite Centre (URSC), Bengaluru

Participants: 126

Semester/Section: 7th Semester ECE Students Organized

by:

IEEE Circuits and Systems Society (CASS)

The Institution of Engineers (IEI)

Indian Society for Technical Education (ISTE)

Institution’s Innovation Council (IIC)

Department of Electronics and Communication Engineering

B.N.M. Institute of Technology (Autonomous), Bengaluru

Staff Coordinators:

Dr. Yasha Jyothi M. Shirur, Faculty Advisor-CASS, HOD, Dept. of ECE, BNMIT

Dr. Jyoti R Munavalli, Faculty Advisor-SPS, Prof. & Head, ED Cell, BNMIT

Dr. Smitha Gayathri D, Associate Professor, Dept. of ECE, BNMIT

Dr. Ashwini S Savanth, IEI Coordinator, Associate Professor, Dept. of ECE, BNMIT

Prof. Sumathi A, ISTE Coordinator, Assistant Professor, Dept. of ECE, BNMIT

Prof. Kiran K N, IIC Coordinator, Assistant Professor, Dept. of ECE, BNMIT

Overview :

The Department of Electronics and Communication Engineering at B.N.M. Institute of Technology (BNMIT), Bengaluru, organized a Field/Exposure Visit to the ISRO U R Rao Satellite Centre (URSC), Bengaluru, on 19th June 2026. The visit was organized in association with the IEEE Circuits and Systems Society (CASS), The Institution of Engineers (IEI), the Indian Society for Technical Education (ISTE), and the Institution's Innovation Council (IIC). The visit provided students with valuable exposure to India's space research activities and helped them understand the practical application of electronics and communication engineering in space missions.

Event Proceedings :

1. The Field/Exposure Visit to ISRO U R Rao Satellite Centre (URSC), Bengaluru, was organized with the objective of bridging the gap between theoretical knowledge and real-world engineering applications. The visit provided students with an opportunity to experience the working environment of one of India's premier space research organizations.

2. The students and faculty members departed from the BNMIT campus at 8:30 AM and arrived at the ISRO U R Rao Satellite Centre, Kodihalli, Bengaluru. Upon arrival, the group was received by ISRO officials who guided the students through various sections of the facility. The visit included audio-visual presentations, interactive discussions and live demonstrations.

3. One of the major highlights of the visit was the screening of a documentary on the making of Chandrayaan-2, India's second lunar exploration mission. The documentary provided students with insights into the conception, design and execution of the mission, including the integration of the Orbiter, Lander Vikram and Rover Pragyan.

4. The documentary also highlighted the engineering challenges involved in satellite fabrication and testing, along with the role of communication systems and electronics in real-time mission control. Students were also introduced to the scientific data obtained from the Chandrayaan-2 mission.

5. ISRO scientists and engineers conducted an informative discussion on India's upcoming and ongoing space missions. The session covered Gaganyaan, future lunar exploration missions, NISAR, Aditya-L1, and future commercial satellite launches under the NewSpace India Limited (NSIL) initiative.

6. The discussion on the Gaganyaan mission provided students with an understanding of India's human spaceflight programme, including the objectives of the mission, astronaut selection and training, and the engineering aspects of the Crew Module and Service Module. The role of communication and embedded systems in ensuring crew safety was also emphasized.

7. The visit included three live demonstrations conducted by ISRO engineers. The first demonstration focused on the Satellite Antenna Tracking System, where students observed ground-based antenna systems used for tracking satellites and learned about signal processing, Sband and X-band frequency bands, and satellite communication.

8. The second demonstration focused on the Environmental Testing of Satellite Components. Students observed the thermal vacuum chamber and vibration testing setup used to simulate the harsh conditions of outer space. The demonstration highlighted the importance of quality assurance and materials engineering in ensuring satellite reliability and longevity.

9. The third demonstration provided students with a guided view of the Clean Room Facility and Satellite Integration process. The scientific staff explained the assembly and integration of satellite subsystems and highlighted the importance of precision electronics, VLSI components and embedded systems in satellite integration.

10. The visit helped students understand how subjects such as signal processing, antenna design, embedded systems and communication theory are directly applied in real-world space missions. The practical demonstrations provided exposure that is not ordinarily available in a classroom environment.

11. Interaction with ISRO scientists encouraged students to explore research careers, postgraduate studies and opportunities in organizations involved in space and defence technology. The visit also reinforced the importance of multidisciplinary collaboration, precision engineering and adherence to quality standards in large-scale engineering projects.

12. The visit was coordinated by the faculty members of the Department of Electronics and Communication Engineering at BNMIT. The coordinators ensured smooth logistics, student discipline and a structured itinerary that maximized the educational value of the visit.

Objective:

The primary objectives of the visit were to:

- Provide students with exposure to satellite communication technologies and space research activities at URSC.
- Motivate students by providing exposure to live demonstrations and developments in space technology.
- Provide an understanding of real-time engineering challenges involved in satellite design, fabrication, testing and deployment.
- Help students appreciate the role of Electronics and Communication Engineering in national space missions.
- Encourage students to explore careers in space research and technology development organizations such as ISRO.

Conclusion:

The Field/Exposure Visit to ISRO U R Rao Satellite Centre (URSC) was an exceptionally enriching experience for the 7th Semester ECE students of BNMIT. The visit provided students with valuable exposure to satellite technology, space research and real-world engineering applications through the Chandrayaan-2 documentary, discussions on the Gaganyaan mission and other future space programmes, and three live demonstrations conducted by ISRO engineers. The experience broadened students' understanding of electronics and communication engineering applications in space technology and motivated them to explore research and higher education opportunities.

Event Images :

Figure 1: Group photograph of 7th Semester ECE students and faculty coordinators at the ISRO U R Rao Satellite Centre (URSC), Bengaluru, following the Field/Exposure Visit on 19th June 2026.

BNM Institute of Technology

An autonomous Institution under VTU

Title of the Event: “Defuse the Bomb”

Date: 30th May, 2026 Time: 9:00 AM to 3:00 PM

Venue: S003

Participants: 75

Organized by:

Team HashVault – Cybersecurity Club, BNMIT

IEEE Circuits and Systems Society (IEEE CASS) – BNMIT

As part of COMET Club Day

Overview :

“Defuse the Bomb” was an interactive team-based technical challenge organized by Team HashVault and IEEE CASS BNMIT as part of COMET Club Day. The event was designed to test participants’ logical reasoning, cryptography, system-analysis and teamwork skills through a multi-stage challenge involving a custom-built simulated electronic device. Participants worked collaboratively to solve clues and complete the different stages within a limited time.

Event Proceedings :

1. The event was organized as an immersive and interactive technical challenge that required participants to work collaboratively to complete multiple stages within a limited time. The activity combined logical reasoning, cryptography, system analysis and teamwork to create an engaging technical learning experience.

2. The event commenced with the registration of participating teams, followed by a briefing on the rules, objectives and safety guidelines of the challenge. Participants were introduced to the simulated bomb device and provided with a Bomb Defusal Manual containing the instructions, clues and protocols required to navigate the different stages.

3. The first stage of the challenge focused on wire rerouting and signal interpretation. Participants analyzed LED indicators and followed the instructions provided in the manual to determine the required connections. This stage tested their attention to detail, logical reasoning and ability to interpret technical documentation accurately.

4. The second stage involved a cryptographic sequencer challenge in which participants used joystick controls to identify hidden signal coordinates and reveal coded information. Teams had to interpret clues, monitor device feedback and complete the sequence within the allotted time.

5. Throughout the challenge, participants actively collaborated with their teammates, discussed possible solutions and adapted their strategies while working under time pressure. The competitive format encouraged effective communication, critical thinking and quick decision-making.

6. The custom-built device and the detailed Bomb Defusal Manual provided participants with an immersive learning experience. The multi-stage nature of the challenge encouraged teams to approach problems systematically while making effective use of the information available to them.

7. Participants demonstrated a high level of enthusiasm and engagement throughout the event. Teams worked together to analyze clues, interpret the manual and solve the challenges within the given time limit, resulting in an energetic and interactive atmosphere.

8. The event concluded with the successful completion of the challenges by participating teams, followed by result announcements and interactions with the organizing team. The activity provided an effective combination of technical problem-solving, teamwork and experiential learning.

9. The event also encouraged participants to develop stronger problem-solving abilities and analytical thinking while working under pressure. The practical and competitive nature of the activity helped students apply logical and technical concepts in an engaging environment.

Objective :

- The primary objectives of the event were to:
- Develop logical reasoning and analytical problem-solving skills among participants.
- Provide an interactive platform to apply concepts related to cryptography and system analysis.
- Encourage teamwork and effective communication while solving technical challenges.
- Develop quick decision-making abilities under time constraints.
- Provide students with an engaging and experiential technical learning environment.
- Encourage participants to approach complex problems systematically and collaboratively.

Conclusion :

The “Defuse the Bomb” event was successfully conducted as part of COMET Club Day and provided participants with a unique and engaging technical problem-solving experience. By combining logical reasoning, cryptography, teamwork and system-analysis challenges, the event encouraged active learning in an interactive environment. The enthusiasm displayed by participants and the smooth execution of the competition contributed significantly to its success. A total prize pool of ₹3,500 was awarded to the top three teams based on their performance. Overall, the event successfully demonstrated how technical concepts can be transformed into an enjoyable and immersive learning experience.

Event Images :

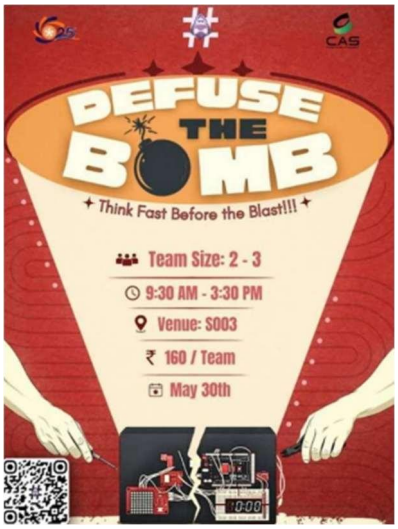

Figure 1: Participants working collaboratively on the simulated device during the challenge.

BNM Institute of Technology

An autonomous Institution under VTU

Title of the Event: "Alumni Series Talk on Ethical Issues in Vision AI"

Date: 17th April, 2026 Time: 11:30 AM to 1:30 PM

Venue: N401, New Building, BNMIT

Participants:120

Semester/Section: 4th Semester

Organized by:

Department of Electronics & Communication Engineering

IEEE Nanotechnology Council

IEEE Circuits and Systems Society (IEEE CASS)

IEEE Signal Processing Society

Staff Coordinators:

Dr. Vrunda Kusanur

Dr. Priyadarshini K Desai

Dr. Yasha Jyothi M. Shirur

Overview :

The Department of Electronics and Communication Engineering at B.N.M. Institute of Technology organized an Alumni Series Talk on “Ethical Issues in Vision AI” on 17th April 2026 in association with the IEEE Circuits and Systems Society, IEEE Nanotechnology Council, and IEEE Signal Processing Society. The session aimed to connect academic learning with realworld technological developments through meaningful interaction with an accomplished alumnus. The event focused on the growing importance of ethical considerations in Artificial Intelligence, particularly in the field of computer vision.

Event Proceedings :

1. The Alumni Series Talk on “Ethical Issues in Vision AI” was organized to create awareness among students about the ethical challenges associated with the rapid advancement of Artificial Intelligence, particularly in the field of computer vision. The session highlighted the importance of considering ethical and societal aspects alongside technical development.

2. The session was delivered by Mr. Suchit Shavi, Head of Research and Development at OpenAI India, who is an alumnus of BNMIT with extensive experience in Artificial Intelligence. He shared valuable insights into ethical decision-making in AI development and emphasized the importance of designing AI systems that are fair, inclusive and trustworthy.

3. During the session, the speaker discussed important ethical concerns associated with Vision AI, including data privacy, algorithmic bias, lack of transparency and accountability in AI systems. Students were introduced to the challenges involved in developing and deploying intelligent systems responsibly.

4. The talk also addressed the societal implications of AI-driven technologies such as facial recognition and surveillance systems. The discussion helped students understand how these technologies can raise concerns related to privacy, fairness and responsible use.

5. The session emphasized the importance of responsible AI practices and ethical decision-making while designing intelligent systems. Students were encouraged to look beyond technical implementation and consider the broader societal consequences of the technologies they develop.

6. The interaction with an accomplished alumnus helped bridge the gap between academic learning and industry practices. Students gained real-world insights into AI research and development and were encouraged to understand the importance of responsible innovation in professional environments.

7. The session was interactive, with students actively participating in discussions and raising thoughtful questions. This interaction helped students gain a deeper understanding of the ethical dimensions of modern technology and encouraged them to approach technological innovation from a balanced perspective.

8. The event also encouraged students to develop critical thinking skills and remain informed about evolving standards and regulations related to Artificial Intelligence. The discussion highlighted the need for technically competent engineers who are also ethically conscious and socially responsible.

Objective :

- The primary objectives of the event were to:
- Create awareness about ethical challenges associated with Artificial Intelligence and Vision AI.
- Help students understand issues related to data privacy, algorithmic bias, transparency and accountability.
- Highlight the societal implications of AI-driven technologies such as facial recognition and surveillance.
- Bridge the gap between academic learning and industry practices through interaction with an accomplished alumnus.
- Encourage responsible innovation and ethical decision-making in AI development.
- Develop critical thinking and ethical awareness among students.
- Motivate students to contribute towards the development of fair, trustworthy and inclusive technologies.

Conclusion :

The Alumni Series Talk on “Ethical Issues in Vision AI” was a highly insightful and impactful session that highlighted the importance of integrating ethical considerations into technological advancement. The event provided students with a deeper understanding of privacy, bias,

transparency and accountability in Vision AI and emphasized the need for responsible and socially conscious innovation. The interaction with an experienced alumnus provided valuable industry insights and encouraged students to balance technical expertise with ethical awareness in their future careers.Event

Images :

Figure 1: Group photograph of students, faculty members and organizers during the event.

BNM Institute of Technology

An autonomous Institution under VTU

Title of the Event: “Avinya 2026 – Project Exhibition”

Date: 11th April, 2026

Time: 9:30 AM

Venue: N502 & N505, New Building, BNMIT

Participants: 120

Semester/Section: ECE Students

Organized by:

Department of Electronics and Communication Engineering

B.N.M. Institute of Technology (Autonomous), Bengaluru

In Association with:

IEEE Circuits and Systems Society (IEEE CAS)

IEEE Nanotechnology Council

The Institution of Engineers (India) – IEI

Staff Coordinators:

Dr. Ashwini Savanth, Associate Professor, Dept. of ECE

Dr. Sujaya B. L., Associate Professor, Dept. of ECE

Overview :

The Department of Electronics and Communication Engineering at B.N.M. Institute of Technology (BNMIT), Bengaluru, organized “Avinya 2026 – Project Exhibition”, providing a platform for ECE students to showcase their technical expertise, innovative ideas and project execution capabilities. The exhibition focused on emerging areas of electronics and communication engineering and encouraged students to address contemporary engineering challenges through practical and innovative solutions.

Event Proceedings :

1. Avinya 2026 – Project Exhibition was organized by the Department of Electronics and Communication Engineering, BNMIT, to provide students with a dynamic platform to demonstrate their technical expertise, innovative thinking and project execution capabilities. The exhibition highlighted the creativity and technical proficiency of students through projects addressing modern engineering challenges.

2. The event encouraged students to move beyond conventional textbook learning and develop innovative solutions in emerging areas of engineering. Projects explored domains such as Edge AI, Industrial IoT and Smart Communication, enabling students to understand and address contemporary technological challenges.

3. The exhibition provided students with hands-on experience in areas including complex circuit design, real-time coding and hardware-software co-design. This practical approach helped students transform theoretical concepts and mathematical models into functional prototypes while gaining experience across different stages of project development.

4. The event also emphasized research-oriented and analytical thinking. Students carried out literature surveys and competitive benchmarking to identify existing technological gaps and develop technically sound project architectures supported by research.

5. Avinya 2026 encouraged collaborative learning and teamwork. Students worked in teams and gained experience in project management, resource allocation, coordination and leadership, reflecting the collaborative environment of professional research and development organizations.

6. The exhibition was organized in association with professional bodies including the IEEE Nanotechnology Council, IEEE Circuits and Systems Society (CAS), and The Institution of Engineers (India) – IEI. Their association added technical value to the event and contributed towards strengthening industry-academia interaction.

7. The event commenced at 9:30 AM in Rooms N502 and N505 of the New Building at BNMIT. The inauguration was graced by Sri. Narayan Rao R. Maanay, Secretary, BNMIT; Prof. T. J. Rama Murthy, Director, BNMIT; Dr. S. Y. Kulkarni, Advisor & Principal, BNMIT; Prof. Eishwar N.
Maanay, Dean, BNMIT; and Dr. Krishnamurthy G. N., Deputy Director, BNMIT.

8. The dignitaries emphasized the importance of applied learning and project-based education and encouraged students to explore entrepreneurial opportunities through their innovative ideas.

9. The exhibition featured projects developed by ECE students across diverse technological domains, including Embedded Systems, VLSI Design, Signal Processing, IoT and Smart Devices, Wireless Communication, AI and Machine Learning Applications in ECE, and Robotics and Automation.

10. The projects were evaluated by a panel comprising industry experts and faculty members based on criteria such as innovation, technical complexity, societal impact and presentation. The evaluator panel included Mr. Venkatesh Murthy Muthigi, Mr. Santhosh M. S., Dr. A. B. Kalpana and Dr. Leelavathi H. P.

11. The evaluation provided students with valuable exposure to professional expectations and constructive feedback from experienced professionals. The interaction helped students understand the importance of scalability, reliability, technical quality and effective communication while presenting engineering solutions.

12. The exhibition also helped students develop communication and professional presentation skills. Participants explained their projects to expert evaluators and demonstrated their ability to communicate technical concepts effectively. The photographs in the report document students presenting and explaining their projects during the exhibition.

13. The successful execution of Avinya 2026 was supported by the event convenors, Dr. Yasha

Jyothi M. Shirur, Professor & HoD, Dept. of ECE, and Dr. Bindu S., Professor, Dept. of ECE, along with coordinators Dr. Ashwini Savanth and Dr. Sujaya B. L.

Objective :

1. The primary objectives of the exhibition were to:
2. Provide ECE students with a platform to demonstrate their technical expertise and innovative ideas.

3.Encourage students to develop creative engineering solutions for contemporary challenges.
4.Develop practical proficiency in circuit design, coding and hardware-software integration.
5.Promote research-oriented thinking through literature surveys and technical analysis.
6.Encourage teamwork, leadership, project management and collaborative learning.
7.Provide exposure to industry expectations and professional standards through expert evaluation.
8.Encourage students to explore entrepreneurial opportunities and the societal impact of engineering solutions.
9.Develop students' technical communication and professional presentation skills.

Conclusion :

Avinya 2026 – Project Exhibition was successfully conducted as a platform showcasing the technical ingenuity, creativity and problem-solving abilities of ECE students. By encouraging students to apply engineering principles to real-world challenges, the exhibition effectively bridged the gap between academic learning and professional practice. The interaction with industry experts and faculty members provided valuable technical feedback and exposure to professional standards. The event also encouraged students to explore research, higher education, entrepreneurship and industry-oriented career opportunities. Overall, Avinya 2026 contributed significantly to experiential learning and the development of industry-ready engineering graduates.

Event Images :

Figure 1: Students presenting their projects during the exhibition.

Figure 2: Students interacting with faculty members and evaluators during the project evaluation.

BNM Institute of Technology

An autonomous Institution under VTU

Title of the Event: “Robo-Track”

Date: 26th March, 2026 Time: 9:00 AM to 1:00 PM

Venue: Ground, BNMIT

Participants:71

Semester/Section: All Semesters

Organized by:

IEEE RAS, IEEE CASS and Robohawks Club

Department of Electronics & Communication Engineering B.N.M. Institute of Technology (Autonomous), Bengaluru

Overview :

The Department of Electronics and Communication Engineering, BNMIT, organized the event “Robo-Track” under IEEE RAS, IEEE CASS and Robohawks Club. The event was conducted with the aim of assessing and enhancing students' skills in robot design, control systems, real-time navigation, embedded systems and mechanical design. The competition provided students with an opportunity to apply their theoretical knowledge to practical robotic implementation.

Event Proceedings :

1. The event “Robo-Track” was organized with the objective of providing students with a practical and challenging platform to demonstrate their knowledge and skills in robotics, embedded systems, mechanical design and control systems.

2. The competition involved participants operating their robots on a predefined track consisting of straight paths, curves, ramps and task-based obstacles. The event evaluated not only the speed of the robots but also the precision and control demonstrated by the participants during navigation.

3. Participants were required to complete two laps within a specified time limit of five minutes. This requirement tested their ability to effectively control and navigate their robots while following the prescribed track and event rules.

4. An important feature of the competition was the inclusion of task-based challenges. Participants were required to knock down at least four out of six bottles placed on the track. This added complexity to the competition and required participants to demonstrate accurate robot control and effective navigation strategies. Failure to achieve this criterion resulted in disqualification.

5. To maintain fairness and consistency throughout the competition, specific rules were established. Participants were allowed a maximum of three hand touches, and these were permitted only when the robot moved outside the track. Participants were also required to complete the entire track without missing any designated sections.

6. The track included ramps with varying levels of difficulty, which added an additional challenge for the participants. A penalty system was implemented for errors made on the ramps. A 10-second penalty was imposed for mistakes on Ramp 1, while a 20-second penalty was imposed for mistakes on the tricky ramp. These penalties were added to the overall completion time.

7. The judging of the competition was primarily based on the total time taken by the participants to complete both laps. In addition to completion time, factors such as task

completion, accuracy of control and adherence to the event rules were also considered during evaluation.

8. The event provided students with an opportunity to apply their theoretical knowledge in a practical environment. Participants were required to demonstrate effective control, precision and consistency while overcoming the different challenges incorporated into the track.

9. Overall, the event successfully engaged students and encouraged them to develop practical skills in robotics. The challenging track, task-based obstacles and penalty system provided an effective platform for students to demonstrate their technical knowledge, problem-solving abilities and robotic control skills.

Objective :

- The primary objectives of the event were to:
- Assess students' practical skills in robot design, control systems and real-time navigation.
- Provide hands-on exposure to robotics, embedded systems and mechanical design.
- Evaluate precision, speed and control while operating robots on a challenging track.
- Encourage students to apply theoretical knowledge to practical robotic implementation.
- Promote experiential learning, technical excellence and problem-solving skills among students.

Conclusion :

The “Robo-Track” event was successfully conducted and provided students with an engaging platform to gain practical experience in robotics. The competition effectively tested participants' abilities in robot control, navigation, precision and task completion while encouraging them to apply their theoretical knowledge to real-world challenges. The event successfully fulfilled its objective of promoting experiential learning and technical excellence among students.

Event Images:

Figure 1: Participants and organizers during the Robo-Track event, with the competition track and robotic obstacles visible at the venue.

BNM Institute of Technology

An autonomous Institution under VTU

Title of the Event: “Robo Knockout”

Date: 25th March, 2026 Time: 12:00 PM to 5:00 PM

Venue: S Block Basement, BNMIT

Participants: 151 Semester/Section: All Semesters

Organized by:

IEEE Robotics and Automation Society (IEEE RAS)

IEEE Circuits and Systems Society (IEEE CASS) B.N.M. Institute of Technology (Autonomous), Bengaluru

Overview :

The Department of Electronics and Communication Engineering, BNMIT, in association with IEEE RAS and IEEE CASS, organized the event “Robo Knockout” as an engaging and competitive robotics event. The event provided students with an opportunity to test their robotic cars in a real-time battle environment while applying their knowledge of robotics, mechanics and control systems in a practical setting.

Event Proceedings :

1. The event “Robo Knockout” was organized with the aim of providing students with practical exposure to robotics and real-time control systems through a competitive and experience-oriented format.

2. The main concept of the event involved two robotic cars competing against each other within an arena. Participants were required to operate and control their robots effectively while attempting to score points through their performance during the battle.

3. The competition was conducted in a knockout format, where two teams competed against each other in every round. Each match was conducted for a duration of three minutes, during which participants attempted to score maximum points through effective hits, movement control and overall robot performance within the arena.

4. At the end of each round, the scores of both teams were compared and the team with the higher score was declared the winner. The winning team advanced to the next round, and the elimination process continued until the final winner was determined.

5. The event maintained a high level of energy and enthusiasm throughout the competition. Participants demonstrated their creativity, technical skills, control strategies and competitive spirit while operating their robotic vehicles in the arena.

6. The event also provided students with an opportunity to observe and learn from the designs, strategies and approaches adopted by other participating teams. This encouraged participants to improve their understanding of robotic design, stability, control and performance.

7. Through direct participation, students gained valuable hands-on experience in controlling and operating robotic vehicles in a competitive environment. They developed a better understanding of important aspects such as stability, control and design efficiency in robotics.

8. The competition also helped students enhance their problem-solving and strategic thinking abilities, as participants were required to make quick decisions during the matches. The event encouraged teamwork and coordination among team members while exposing students to challenges commonly encountered in robotics competitions.

9. Overall, the event successfully combined technical learning with competition and provided students with a practical platform to test their ideas, improve their skills and gain confidence in working with robotic systems.

Objective :

The primary objectives of the event were to:

- Provide students with practical exposure to robotics and real-time control systems.
- Encourage participants to design and operate efficient robotic vehicles.
- Develop strategic thinking and quick decision-making abilities among students.
- Improve students' understanding of robotic stability, control and design efficiency.
- Encourage teamwork, coordination and problem-solving through competitive robotics.
- Create an experience-oriented learning environment that promotes interest in robotics.

Conclusion :

The “Robo Knockout” event was successfully conducted as an exciting and informative robotics competition. It effectively combined technical learning with a competitive environment and provided students with a practical platform to test their ideas and improve their robotic control skills. The event received a positive response from the participants and successfully achieved its objective of promoting hands-on learning and interest in robotics. Overall, the event contributed to the development of both technical and interpersonal skills among students.

Event Images :

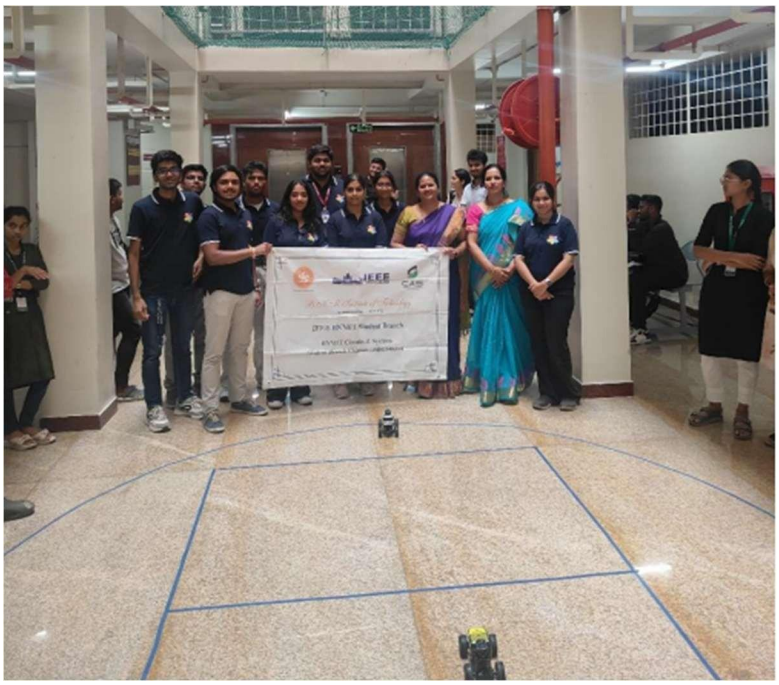

Figure 1: Group photograph of the organizing team and participants with the event banner at the competition venue.

BNM Institute of Technology

An autonomous Institution under VTU

Title of the Event: “Industrial Visit to IISc on Open Day 2026”

Date: 7th March, 2026 Time: 10:00 AM to 5:00 PM

Venue: Indian Institute of Science (IISc), Bangalore

Participants: 30

Semester/Section: 4th and 6th Semester ECE Students

Organized by:

IEEE Circuits and Systems Society (IEEE CASS)

IEEE Robotics and Automation Society (IEEE RAS) B.N.M. Institute of Technology (Autonomous), Bengaluru

Staff Coordinators:

Dr. Yasha Jyothi M Shirur, HoD of Dept. of ECE

Dr. Rekha P, Professor, Dept. of ECE

Overview :

The industrial visit to the Indian Institute of Science (IISc), Bangalore was successfully organized by CASS BNMIT during its Open Day, with the objective of providing students exposure to advanced research facilities and innovations in science and technology. The visit was arranged to help students gain insights into real-world applications of engineering concepts and explore ongoing research activities at one of India's premier research institutions.

Event Proceedings :

1. The industrial visit to the Indian Institute of Science (IISc), Bangalore was organized during its Open Day to provide students with an opportunity to explore one of India's leading research institutions. The visit focused on exposing students to advanced research facilities, innovative technologies and ongoing developments in science and engineering.

2. During the visit, students had the opportunity to explore various laboratories, research exhibits and demonstrations presented by different departments of IISc. Research scholars and faculty members showcased innovative projects and experimental setups, providing students with valuable exposure to ongoing research activities.

3. Participants observed demonstrations related to robotics, electronics, artificial intelligence and other emerging technologies. Researchers explained the working principles, applications and significance of their projects, helping students understand how theoretical concepts learned in classrooms are implemented in real-world research and development.

4. The visit also provided students with an opportunity to interact with researchers, faculty members and scholars. These interactions helped participants gain insights into ongoing advancements in science and engineering and understand the importance of research and innovation in technological development.

5. The Open Day provided an enriching academic and research environment where students could observe innovative projects and experimental setups directly. The demonstrations helped bridge the gap between theoretical learning and practical implementation.

6. The visit encouraged students to develop greater interest in research, innovation and higher studies. Exposure to the research environment at IISc motivated participants to explore opportunities in science and technology and consider research-oriented academic and professional careers.

7. Overall, the visit was highly informative and motivating, giving students a deeper appreciation for advanced research, technological innovation and the practical application of engineering concepts.

Objective :

- The primary objectives of the visit were to:
- Provide students exposure to the research environment and advanced technological developments at the Indian Institute of Science (IISc), Bangalore.
- Help students understand the practical applications of engineering and scientific concepts through live demonstrations and research exhibits.
- Encourage interaction with researchers and scholars and provide insights into ongoing research and innovation.
- Inspire students to explore higher studies, research opportunities and careers in science and technology.

Conclusion:

The industrial visit to the Indian Institute of Science (IISc), Bangalore on its Open Day was a highly informative and enriching experience for the students. The visit provided valuable exposure to advanced research, innovative technologies and real-world applications of engineering concepts. It also motivated students to develop curiosity towards research and higher studies. Overall, the visit successfully broadened students' understanding of scientific

advancements and inspired them to pursue innovation in their academic and professional journeys.

Event Images :

Figure 1: Group photograph captured at the Indian Institute of Science, Bangalore, with the location details visible.

BNM Institute of Technology

An autonomous Institution under VTU

Title of the Event: “Rig to Solder”

Date: 18th February, 2026 Time: 10:00 AM to 5:00 PM

Venue: N603, BNMIT

Participants: 60

Semester/Section: 4th & 6th Semester + 10th Std Students

Organized by:

IEEE Circuits and Systems Society (IEEE CASS)

IEEE Robotics and Automation Society (IEEE RAS)

Robohawks Club

B.N.M. Institute of Technology (Autonomous), Bengaluru

Overview :

The Department of Electronics and Communication Engineering, BNMIT, organized “Rig to Solder” in collaboration with the IEEE Robotics and Automation Society (RAS), IEEE Circuits and Systems Society (CASS), and Robohawks Club. The event was conducted with the objective of providing students with hands-on experience in electronics circuit building and PCB soldering. The session focused on strengthening students’ practical knowledge of hardware implementation and helping them understand the transition from theoretical circuit concepts to real-world applications.

Event Proceedings:

1. The event “Rig to Solder” was organized with the aim of providing students with practical exposure to circuit building and PCB soldering. The session focused on strengthening students’ practical knowledge in hardware implementation and helping them understand the importance of proper soldering techniques.

2. The event began with an introduction to basic electronic components and the importance of soldering in circuit design and hardware implementation. The organizers explained the various tools used during soldering, including the soldering iron and solder wire, along with the necessary safety precautions to be followed while working with the equipment.

3. Participants were initially provided with resistors to practice soldering on PCB boards. The organizers explained the correct soldering procedure and guided the students throughout the activity. Participants practiced the techniques demonstrated during the session and clarified their doubts with the organizers.

4. Following the initial practice session, participants were provided with pre-packed PCB soldering kits. The kits were categorized into different levels based on their complexity, with

each kit containing the required electronic components and a PCB board designed for practical assembly.

5. Participants picked slips through which the topics and corresponding PCB kits were assigned to them. They were then instructed on the appropriate soldering procedure and were given the opportunity to assemble the circuits practically using the components provided.

6. The event created an interactive learning environment where students gained practical exposure to soldering techniques and learned about common mistakes such as improper solder joints and excess soldering. The guided practice helped participants develop confidence in handling soldering equipment and electronic components.

7. Through the practical activities, students gained experience in soldering electronic components on PCB boards using the pre-packed PCB kits provided during the event. The categorized kits also helped students understand structured circuit assembly and improve their hands-on technical skills.

8. The event helped students understand the importance of clean and secure solder joints while strengthening their foundational knowledge of electronics. The practical experience gained during the session is useful for academic laboratory work as well as future hardware-based projects.

Objective :

- The primary objec ves of the event were to:
- Provide prac cal exposure to circuit design and implementa on.
- Teach students the transi on from breadboard (rig) to soldered PCB circuits.
- Enhance understanding of basic electronic components and their working.
- Familiarize students with soldering tools, materials and safety precau ons.
- Develop students' prac cal skills in PCB assembly and soldering.
- Build confidence among students in handling electronic components and soldering equipment.

Conclusion :

The “Rig to Solder” event was an engaging and informative activity that successfully enhanced students’ practical electronics skills. The collaboration between IEEE Robotics and Automation Society (RAS), IEEE Circuits and Systems Society (CASS), and Robohawks Club ensured smooth execution and effective learning. The event received positive feedback from participants and successfully achieved its objective of strengthening students’ foundational soldering skills and practical understanding of electronics.

Event Images :

Figure 1: Event poster and photographs showcasing the practical activities conducted during “Rig to Solder”.

BNM Institute of Technology

An autonomous Institution under VTU

Title of the Event: “Future of Automotive: How E/E Architecture is Powering the Shift to Software-Defined Vehicles”

Date: 14th February, 2026 Time: 11:00 AM to 12:30 PM

Venue: N401 Seminar Hall, BNMIT

Participants:66

Semester/Section: IV & VI A & B

Organized by:

Department of Electronics and Communication Engineering

IEEE Circuits and Systems Society

IEEE Nanotechnology Council

B.N.M. Institute of Technology (Autonomous), Bengaluru

Staff Coordinators:

Dr. Yasha Jyothi M. Shirur, Professor and Head, ECE

Dr. Smitha Gayathri D, Associate Professor, ECE

Prof. Sarala T, Assistant Professor, ECE Overview :

The Department of Electronics and Communication Engineering, B.N.M. Institute of Technology, in association with the IEEE Circuits and Systems Society and IEEE Nanotechnology Council, organized a Technical Talk titled “Future of Automotive: How E/E Architecture is Powering the

Shift to Software-Defined Vehicles" on 14th February 2026 at N401 Seminar Hall. The session was organized to expose students and faculty to emerging trends in automotive electronics, particularly the evolution of Electrical/Electronic (E/E) architecture and its role in enabling software-defined vehicles.

The session was delivered by Mr. Rajesh, Principal Engineer at Intel, who shared insights from industry practices, current research directions and future technological transformations in automotive systems.

Event Proceedings :

1. The technical talk was organized with the objective of providing students and faculty with an understanding of emerging developments in automotive electronics and the transition towards software-defined vehicles. The session focused on the evolution of Electrical/Electronic architecture and its increasing importance in modern automotive systems.

2. The resource person, Mr. Rajesh, Principal Engineer at Intel, shared insights from industry practices, current research directions and future technological developments in automotive systems. The session helped participants gain an understanding of the technological changes taking place in the automotive electronics domain.

3. The speaker explained the transition from hardware-centric automotive design to softwaredefined architectures. The discussion highlighted how software is becoming increasingly important in determining vehicle functionality and enabling advanced features in modern automobiles.

4. The session highlighted the importance of centralized computing platforms in modern vehicles. Students were introduced to the changing architecture of automotive electronic systems and the role of powerful computing platforms in supporting increasingly complex vehicle functionalities.

5. The resource person also discussed the role of embedded systems, communication networks and Artificial Intelligence (AI) in next-generation mobility. The session helped students

understand how multiple technological domains are integrated to develop advanced automotive systems.

6. The talk also focused on the changing skill requirements in the automotive electronics industry. The speaker emphasized the importance of interdisciplinary knowledge in embedded systems, software engineering and communication protocols for engineers aspiring to work in this domain.

7. The session was highly interactive, with students actively participating in the question-andanswer discussion. Students had the opportunity to clarify their doubts and gain further insights into automotive technologies and the future direction of the industry.

8. The technical talk provided participants with valuable exposure to real-world automotive system design and current industry trends. The interaction with an industry expert helped students understand the practical applications of concepts related to electronics, embedded systems and communication technologies.

9. The session also provided students with greater clarity regarding career opportunities in automotive electronics, embedded systems and software-defined vehicle platforms. The discussion encouraged students to explore advanced technological and research areas related to future mobility.

10. Overall, the technical talk successfully strengthened industry-academia interaction and provided students with an opportunity to understand the technological transformation taking place in the automotive sector.

Objective :

- The primary objectives of the technical talk were to:
- Expose students and faculty to emerging trends in automotive electronics.
- Introduce the evolution of Electrical/Electronic (E/E) architecture in modern vehicles.
- Explain the role of E/E architecture in enabling software-defined vehicles. ● Provide insights into centralized computing platforms used in modern automotive systems. ● Highlight the role of embedded systems, communication networks and AI in next-generation mobility.

- Bridge the gap between academic learning and current industry developments.
- Provide students with insights into industry expectations and career opportunities in automotive electronics.
- Encourage students to explore advanced research and technological developments in future mobility.

Conclusion :

The Technical Talk on “Future of Automotive: How E/E Architecture is Powering the Shift to Software-Defined Vehicles” was informative and well-received by both students and faculty. The session provided valuable exposure to real-world automotive system design, emerging E/E architectures and the growing role of software in modern vehicles. The interaction with the industry expert helped students understand current industry trends and career opportunities in automotive electronics, embedded systems and software-defined vehicle platforms. Overall, the event successfully contributed to strengthening industry-academia interaction and enhancing students' technical awareness of emerging automotive technologies.

Event Images :

Figure -1 Industry expert delivering an insightful session on Automotive SOC architecture during the technical talk at BNMIT.

Figure -2 :Students actively engaging with the industry expert during the technical session

BNM Institute of Technology

An autonomous Institution under VTU

Title of the Event: “Roadmap to IITs & PSU Jobs through GATE”

Date: 8th January, 2026 Time: 11:00 AM to 12:30 PM

Venue: N401 Seminar Hall, BNMIT

Participants:62

Semester/Section: VI A & B

Overview :

The Department of Electronics and Communication Engineering, B.N.M. Institute of Technology (BNMIT), Bengaluru, organized an expert talk titled “Roadmap to IITs & PSU Jobs through GATE” on 8th January 2026 at N401 Seminar Hall, in association with the IEEE Circuits and Systems Society and IMS GATE Academy. The session was organized to create awareness among students about the Graduate Aptitude Test in Engineering (GATE) and to provide guidance on higher education opportunities at premier institutions and career opportunities in Public Sector Undertakings (PSUs).

The session was delivered by Mr. Vipin Kumar Mishra, Lead Mentor for GATE Academy, IMS GATE Academy, who provided students with practical guidance on examination preparation, career planning and opportunities available through GATE.

Event Proceedings :

1. The expert talk was organized with the objective of creating awareness among students about the importance of the Graduate Aptitude Test in Engineering (GATE) as a pathway to higher education and career opportunities.

2. The session began with an introduction highlighting the significance of GATE as a gateway to admissions in premier institutions such as IITs and IISc, as well as recruitment opportunities in Public Sector Undertakings.

3. The resource person, Mr. Vipin Kumar Mishra, Lead Mentor for GATE Academy, IMS GATE Academy, provided students with a structured and practical overview of the GATE examination and its relevance to their academic and professional careers.

4. The speaker explained the GATE examination pattern and syllabus, helping students understand the structure of the examination and the areas that need to be covered during preparation.

5. The session highlighted the importance of GATE scores for admissions to IITs, IISc and other premier institutions, providing students with greater awareness of higher education opportunities available through the examination.

6. A detailed preparation roadmap for GATE was discussed. The speaker guided students on how to plan their preparation systematically and emphasized the importance of starting early and maintaining consistency.

7. The session also covered time management strategies and subject-wise planning. Students were provided with guidance on effectively allocating their preparation time and approaching different subjects based on their individual strengths and areas requiring improvement.

8. The speaker discussed common mistakes that students should avoid during GATE preparation. These insights helped participants understand the importance of disciplined preparation and effective examination strategies.

9. The talk also provided information about career opportunities available after qualifying GATE, including opportunities in Public Sector Undertakings, research and higher studies. This helped students understand the different career pathways available through competitive examinations.

10. The resource person shared motivational insights, real-life success stories and preparation tips, encouraging students to set clear academic and professional goals and work towards them through systematic preparation.

11. The session concluded with an interactive question-and-answer segment, during which students actively participated and clarified their doubts regarding preparation strategies, cut-offs and career prospects through GATE.

12. Overall, the session provided students with a clearer understanding of GATE preparation and the opportunities associated with qualifying the examination. It encouraged students to plan their preparation early and approach their academic and career goals in a structured manner.

Objective :

- The primary objectives of the expert talk were to:
- Create awareness among students about the Graduate Aptitude Test in Engineering (GATE).
- Guide students regarding admissions to IITs and other premier institutions.
- Provide insights into career opportunities in Public Sector Undertakings (PSUs).
- Explain the GATE examination pattern and syllabus.
- Provide students with a structured preparation roadmap.
- Introduce effective time management and subject-wise preparation strategies.
- Highlight career opportunities in PSUs, research and higher studies after qualifying GATE.
- Motivate students to plan early and prepare systematically for competitive examinations.
- Help students make informed academic and professional career decisions.

Conclusion :

The expert talk on “Roadmap to IITs & PSU Jobs through GATE” was highly informative and beneficial for the participating students. The session provided a clear understanding of GATE preparation strategies, higher education opportunities at premier institutions and career pathways in Public Sector Undertakings. The interaction with the resource person also helped students gain practical guidance regarding preparation, cut-offs and future career prospects. The Department of Electronics and Communication Engineering, BNMIT, expresses sincere gratitude to IMS GATE Academy and Mr. Vipin Kumar Mishra for their valuable contribution towards making the session informative and beneficial for the students.

Event Images :

Figure 1: Expert session on “Career Opportunities After GATE” being delivered to ECE students as part of the roadmap to IITs and PSU jobs workshop.

Figure 2: Students attentively participating in the expert talk on GATE preparation and career pathways to IITs and PSU jobs during the workshop session.