

B N M Institute of Technology

An Autonomous Institution under VTU. Approved by AICTE

Department: Electronics and Communication Engineering

Scheme of Teaching and Examination - Autonomous Effective from Academic year 2023-24

I Semester M. Tech (VLSI Design and Embedded Systems)

Sl. No.	Course Type	Course Code	Course Title		Teaching Department	Teaching Hours /Week				Hours/ Week	Examination			
						L	T	P	J		Credits	CIA Marks	SEA Marks	Total Marks
1	PCC	23VDE211	ASIC Design		ECE	4	-	-	-	4	4	50	50	100
2	PCI	23VDE212	Real Time Embedded Systems		ECE	3	-	2	-	5	4	50	50	100
3	PCI	23VDE213	CMOS Circuit Design		ECE	3	-	2	-	5	4	50	50	100
4	PBL	23VDE214	Advanced Digital System Design using Verilog		ECE	2	-	2	2	6	4	50	50	100
5	PEC	23VDEP215X	23VDEP2151	Advances in VLSI Design	ECE	3	-	2	-	3	4	50	50	100
	23VDEP2152		Nano Technology											
	23VDEP2153		Internet of Things and its Applications											
6	PCC	23VDE216	Research Methodology & IPR		ECE	2	-	-	-	2	2	50	50	100
TOTAL						17	0	8	2	25	22	300	300	600

L-Theory lecture, T – Tutorial, P – Practical, J – Project NCMC- Non Credit Mandatory Course

CIA: Continuous Internal Assessment, SEA: Semester End Assessment

Note: PCC: Professional Core Course, **HSS:** Humanity and Social Science & Management Courses, **PCI:** Professional Core Integrated

PBL: Project Based Learning **AEC:**Ability Enhancement Courses, **PEC:** Professional Elective, **INT:** Summer Internship, **PRJ:** Project Work

Credit definition: 1 hour Lecture (L) per week = 1 Credit

2 hours Tutorial (T) per week = 1 Credit

2 hours Practical /Drawing (P) per week = 1 Credit

2 hours Project Component (J) per week = 1 Credit

(a) 4 Credit courses are to be designed for 50 hours Teaching – Learning process.

(b) 3 Credit courses are to be designed for 40 hours Teaching – Learning process.

(c) 2 Credit courses are to be designed for 25 hours Teaching – Learning process

(d) 1 Credit course are to be designed for 12-15 hours Teaching – Learning process

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II Semester M. Tech (VLSI Design and Embedded Systems)

Sl. No	Course Type	Course Code	Course Title		Teaching Department	Teaching Hours /Week				Hours/ Week	Examination			
						L	T	P	J		Credits	CIA Marks	SEA Marks	Total Marks
1	PCC	23VDE221	VLSI Testing and Testability		ECE	4	-	-	-	4	4	50	50	100
2	PCI	23VDE222	Low Power VLSI Design		ECE	3	-	2	-	5	4	50	50	100
3	PCI	23VDE223	Design of Analog and Mixed Mode VLSI Circuits		ECE	3	-	2	-	5	4	50	50	100
4	PBL	23VDE224	System Verilog for Verification		ECE	2	-	2	2	6	4	50	50	100
5	PEC	23VDEP225X	23VDEP2251	Reconfigurable Computing	ECE	3	-	-	-	3	3	50	50	100
	23VDEP2252		Static Timing Analysis											
	23VDEP2253		Wearable Technology											
6	PCC	23VDE226	Project Management and Finance		ECE	3	-	-	-	3	3	50	50	100
TOTAL						18	0	6	2	26	22	300	300	600

Summer Internship to be carried out during the vacation between II & III Semester

Summer Internship - I (23VDEI235): All the students registered to II year of MTech shall have to undergo mandatory internship of 4 weeks during II semester or III semester vacation. Semester End Assessment will be conducted in III semester and the prescribed credit will be included. Internship shall be considered as a head of passing and shall be considered for the award of degree. Those, who do not take up / complete the internship shall be declared fail and shall have to complete during subsequent examination after satisfying the internship requirements. (The faculty coordinator or mentor has to monitor the students' internship progress and interact to guide them for the successful completion of the internship.)

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III Semester M. Tech (VLSI Design and Embedded Systems)

Sl. No	Course Type	Course Code	Course Title		Teaching Department	Teaching Hours /Week					Examination			
						L	T	P	J	Hours /Week	Credits	CIA Marks	SEA Marks	Total Marks
1	PCC	23VDE231	CMOS RF Circuits Design		ECE	3	-	-	-	3	3	50	50	100
2	PCC	23VDE232	CAD for Digital Systems		ECE	3	-	-	-	3	3	50	50	100
3	PEC	23VDEP233X	23VDEP2331	VLSI Design for Signal Processing	ECE	3	-	-	-	3	3	50	50	100
	23VDPE2332		Machine Learning using Python	-			-	-						
	23VDEP2333		Synthesis and Optimisation of Digital Circuits	-			-	-						
4	PEC	23VDEP234X	23VDEP234X	MOOC/NPTEL (Subjected to offering by NPTEL)	ECE	3	-	-	-	3	3	50	50	100
5	INT	23VDEI235	Internship			-	-	6	-	6	3	50	50	100
6	PRJ	23VDEJ236	Project Work Phase-1			-	-	-	10	10	5	100	-	100
TOTAL						12	-	6	10	28	20	350	250	600

Summer Internship to be carried out during the vacation between II & III Semester

Summer Internship - I (23VDEI235): All the students registered to II year of M.Tech shall have to undergo mandatory internship of 6 weeks between II semester or III semester vacation. Semester End Assessment will be conducted in III semester and the prescribed credit will be included. Internship shall be considered as a head of passing and shall be considered for the award of degree. Those, who do not take up / complete the internship shall be declared fail and shall have to complete during subsequent examination after satisfying the internship requirements. (The faculty coordinator or mentor has to monitor the students' internship progress and interact to guide them for the successful completion of the internship.)

Project work: Phase-1 (23VDEJ236): Based on the abilities of the students and recommendations of the mentor, a single discipline or a multidisciplinary project can be assigned to an individual student. The progress of the project work will be evaluated continuously. There will be 2 seminars in 2 phases, evaluated by a panel of faculty members with HOD as the Chairperson.

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IV Semester M. Tech (VLSI Design and Embedded Systems)

Sl. No	Course Type	Course Code	Course Title	Teaching Department	Teaching Hours /Week					Examination			
					L	T	P	J	Hours/Week	Credits	CIA Marks	SEA Marks	Total Marks
1	PEC	23VDEP241X	MOOC/NPTEL Self learning courses on latest trends in VLSI and Embedded Area	Online	3	-	-	-	3	3	50	50	100
2	PRJ	23VDEJ242	Project Work Phase-2	ECE	-	-	-	26	26	13	50	50	100
TOTAL					3	-	-	26	29	16	100	100	200

Project work:Phase-2 (23VDEJ242): Based on the abilities of the students and recommendations of the mentor, a single discipline or a multidisciplinary project can be assigned to an individual student. The progress of the project work will be evaluated continuously. There will be 2 seminars in 2 phases and one final presentation with demonstration which are evaluated by a panel of faculty members with HOD as the Chairperson.