Dept. of Electronics and Communication Engineering
M.Tech (VLSI Design and Embedded Systems)
Choice Based Credit System (CBCS and Outcome Based Education (OBE)

Semester: I

Course Name: ASIC DESIGN **Course Code: 23VDE211**

L: T: P: J	**4 : 0 : 0 : 0**	**CIA Marks:** 50
Credits:	**4**	**SEA Marks:** 50
Hours/Week (Total)	**4**	**SEA Duration:** 03 Hours

Pre-Requisites: A Brief History of MOS Transistors, Theory and Fundamentals of Integrated Circuits, Logic Design, Basic of delay calculation and storage elements

Course Learning Objectives: The students will be able to

1	Explore the design flow of different types of ASIC
2	Understand the design of combinational and sequential logic components along I/O cells
3	Calculate the delay and logical effort of the logic circuit
4	Understand the Programmable ASICs Logic Cells
5	Understand the Physical design flow

Module-1: Introduction to ASICs	**No. of Hours**	**Blooms Cognitive Levels**
Types of ASICs: Full Custom ASIC, Semi- custom based ASICS, Standard Cell based ASIC, Gate array-based ASIC, Channeled gate array, Channel less gate array, Structured gate array, Programmable logic devices, FPGA, ASIC Design flow	**10**	**Understand CO1**
Module-2: CMOS Logic		
Combinational logic cells, Sequential logic cells: Latch, flipflop, clocked inverter. **Datapath logic cells:** Data Path Elements, Adders, Multipliers, Arithmetic operator (Practical approach), I/O Cells, Cell Compilers	**10**	**Apply CO2**
Module-3: ASIC Library Design		
Logical Effort: Predicting delay, logical area and logical efficiency, logical paths, multistage cells, optimum delay, optimum number of stages. Library-cell design. **Programmable ASICs:** The Antifuse, Static RAM, EPROM and EEPROM technology	**10**	**Apply CO3**
Module-4: Programmable ASICs logic cells		
Actel ACT: ACT 1 logic module, Shannon's expansion theorem, Multiplexer logic as function generators, Timing model and critical path, Speed grading, Worst-case timing. Programmable ASIC Design Software: Design System, Logic synthesis, Introduction to Synthesis and Simulation. (Practical analysis of the design parameters for speed, area & power optimization). **Low-Level Design Entry:** Schematic Entry: Hierarchical design. The cell library, Names, Schematic Icons & Symbols, Nets, schematic entry for ASIC'S, connections, vectored instances and buses, Edit in place, Attributes, Netlist screener, Back- annotation	**10**	**Apply CO4**
Module-5: Physical Design Flow		
ASIC Construction: Floor Planning and Placement, Routing, Physical Design, CAD Tools, System Partitioning, Estimating ASIC size, Partitioning Methods. Floor planning tools, I/O and power planning, Clock Planning, placement algorithms, iterative placement	**10**	**Understand CO5**

Course Outcomes: After completing the course, the students will be able to	
23VDE211.1	Understand the terminologies associated with standard cells and FPGAs, the issues involved in ASIC Design, including technology choice, design management, tool-flow.
23VDE211.2	Describe the concept of ASIC design methodology and analyze data path elements, logical effort and FPGA architecture
23VDE211.3	Design data path elements for ASIC cell libraries and compute optimum path delay
23VDE211.4	Analyze the design of FPGAs and ASICs suitable for specific tasks perform design entry and explain the physical design flow
23VDE211.5	Create floor plan including placement, partition and routing with the use of CAD algorithms
23VDE211.6	To implement a design of medium complexity (around 20K gates) using ASIC methodologies

Reference Books

1. Application - Specific Integrated Circuits, Michael John Sebastian Smith Addison- Wesley Professional, 2005.
2. CMOS VLSI Design: A Circuits and Systems Perspective Neil H.E. Weste, David Harris,and Ayan Banerjee, Addison Wesley/ Pearson education 3rd edition, 2011.
3. VLSI Design: A Practical Guide for FPGA and ASIC Implementations, Vikram Arkalgud Chandrasetty, Springer, ISBN: 978-1-4614-1119-2. 2011.
4. An ASIC Low Power Primer, Rakesh Chadha, Bhasker J Springer, ISBN: 978-14614-4270-7.

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<tr><td colspan="2">Average of two tests – 25 Marks</td></tr>
<tr><td>Assignment</td><td colspan="2">15</td></tr>
<tr><td>AAT</td><td colspan="2">10</td></tr>
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Dept. of Electronics and Communication Engineering
M.Tech (VLSI Design and Embedded Systems)
Choice Based Credit System (CBCS and Outcome Based Education (OBE)

Semester: I

Course Name: REAL TIME EMBEDDED SYSTEM **Course Code: 23VDE212**

L: T: P: J	**3: 0: 2: 0**	**CIA Marks: 50**
Credits:	**4**	**SEA Marks: 50**
Hours/Week (Total):	**5**	**SEA Duration: 03 Hours**

Pre-Requisites: Embedded System and Operating System, Scheduler Concepts, Hamming Code and Semaphores, Hardware, firmware and software components, and Operating System

Course Learning Objectives: The students will be able to

1	Understand the fundamental concepts of Real Time Embedded System, Real Time Operating System, Real Time Services, Utilities, Resources and Scheduler Concepts.
2	Analyze Static and Dynamic priority scheduling policies, Missed deadlines and QoS.
3	Design ECC memory, Shared memory, critical section, thread safe re-entrant function to handle secure communication and blocking, Deadlock and live lock.
4	Explain the real time embedded components for a system.
5	Apply the knowledge of architecture features of hard RTOS and Open-Source OS tools and platforms for multithreaded programming.

Module-1: Real Time Services and Resources	**No. of Hours**	**Blooms cognitive Levels**
Introduction, A Brief history of Real Time Systems, A brief history of Embedded Systems, Real Time Services, RTS Timeline with and without hardware acceleration, System Resources, Resource Analysis, Real-Time Service Utility, Scheduler Concepts: State transition diagrams and State Transition Table, Real Time Operating System.	**10**	**Understand CO1**
Module-2: Static and Dynamic Priority Scheduling Policies		
Preemptive Fixed Priority Scheduling Policy (Rate Monotonic Policy), Deadline Monotonic Policy, Dynamic priority policies, Missed Deadlines, QoS, Alternatives to RM policy. Necessary and Sufficient Feasibility	**10**	**Apply CO2**
Module-3: Memory and Multi Resource Services		
ECC Memory and design with even and odd parities, Shared Memory, Blocking, Deadlock and live lock, Critical sections to protect shared resources, Priority Inversion. Thread Safe Re-entrant Function	**10**	**Apply CO3**
Module-4: RTES Components for a System		
Introduction, Hardware Components, Stereo Vision Tracking system, Firmware components – Boot code, Device driver and OS Services, RTOS system software mechanisms, Computer Vision Application: Object Tracking and Image Processing for Object recognition Software application components	**10**	**Understand CO4**
Module-5: Real Time Operating System		
Traditional Hard Real Time Operating System Introduction, Evolution of Real Time Scheduling and Resource management, Asymmetric and Symmetric Multicore Processing, Future Directions to RTOS, SMP support models, RTOS Hypervisors, Open Source, RTOS: Free RTOS alternatives, Platforms and tools, Processor Core Affinity and multithreaded	**10**	**Apply CO5**

Sl. N0	Lab Experiments
1	ESP32 Basics- Understanding ESP32 Board and Components, Installing and working with Arduino IDE, Program to read the status of push button & control LED & Buzzer
2	Program to display a message on LCD using ESP32
3	Program to control LED interfaced to ESP32 using Bluetooth (HC-05)
4	Program to control LED interfaced to ESP32 using Wifi (Blynk)
5	Program for creating child threads
6	Programs to build multithreaded applications
7	Program for FIFO scheduling
8	Program for Priority based scheduling
9	Revision
10	Lab Assessment

Course Outcomes: After completing the course, the students will be able to	
23VDE212.1	Understand the fundamental concepts of Real Time Embedded System, RealTime Operating System, Real Time Services, Utilities, Resources and Scheduler Concepts.
23VDE212.2	Analyze Static and Dynamic priority scheduling policies, Missed deadlines and QoS.
23VDE212.3	Design ECC memory, Shared memory, critical section, thread safe re-entrant function to handle secure communication and blocking, Deadlock and livelock.
23VDE212.4	Explain the real time embedded components for a system.
23VDE212.5	Apply the knowledge of architecture features of hard RTOS and Open-source OS tools and platforms for multi-threaded programming.

Reference Books

1. James W. S. Liu, Real Time Systems, Pearson Education, 2008.
2. Dr. K.V.K.K Prasad, Embedded/Real Time Systems, Concepts, Design and Programming, Black Book, Dream Tech Press, New edition, 2010.
3. Sam Siewert, "Real-Time Embedded Systems and Components", Cengage Learning India Edition, 2007.
4. Sam Siewart and James Pratt, Real Time Embedded Components and Systems with Linux and RTOS, Mercury Learning and Information, 2016.

Marks Distribution for Assessment:

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Dept. of Electronics and Communication Engineering M. Tech (VLSI Design and Embedded Systems)		
Semester: I		
Course Name: CMOS Circuit Design		**Course Code: 23VDE213**
L: T: P: J	**3: 0: 2: 0**	**CIA Marks: 50**
Credits	**4**	**SEA Marks: 50**
Hours/Week (Total)	**5 (50)**	**SEA Duration: 03 Hours**

Pre-Requisites: Metal Oxide Semiconductor (MOS) Structure, Inverters, Semiconductor memory, Concept of Pass Transistor and BJTs.

Course Learning Objectives: The students will be able to

1	Explain VLSI Design Methodologies
2	Learn Static and Dynamic operation principles, analysis and design of inverter circuit.
3	Infer state of the art Semiconductors Memory circuits.
4	Outline the comprehensive coverage of Methodologies and Design practice that are used to reduce the Power Dissipation of largescale digital circuits.
5	Illustrate VLSI and ASIC design

Module-1: MOS Transistor and MOS Inverters- Static Characteristics	**No. of Hours**	**Blooms cognitive Levels**
MOS Inverters-Static Characteristics: Introduction, Resistive-Load Inverter, Inverters with n-Type MOSFET Load. CMOS Inverter. Scaling and Small-Geometry Effects. **Lab Experiment: 1**	**10**	Apply CO1
Module-2: MOS Inverters:		
Switching Characteristics and Delay-Time Definition, Calculation of Delay Times, Inverter Design with Delay Constraints, Estimation of Interconnect Parasitics, Calculation of Interconnect Delay, Switching Power Dissipation of CMOS Inverters. **Lab Experiment: 2 & 3**	**10**	Analyze CO2
Module-3: Semiconductor Memories:		
Dynamic Random Access Memory (DRAM), Static Random Access Memory (SRAM), Nonvolatile Memory, Flash Memory & Ferroelectric Random Access Memory (FRAM) **Lab Experiment: 4 & 5**	**10**	Apply CO3
Module-4: Dynamic Logic Circuits		
Dynamic Logic Circuits: Basic Principles of Pass Transistor Circuits, Voltage Bootstrapping, Synchronous Dynamic Circuit Techniques, High Performance Dynamic CMOS circuits **Lab Experiment: 6 & 7**	**10**	Apply CO4
Module-5: BiCMOS Logic Circuits &: Chip Input and Output (I/O) Circuits		
BiCMOS Logic Circuits: Structure and Operation, Dynamic Behavior of BJTs: Basic BiCMOS Circuits: Static Behavior and BiCMOS Applications. ESD Protection, Input Circuits, Output Circuits and L(di/dt) Noise, On Chip Clock Generation and Distribution. **Lab Experiment: 8 to 10**	**10**	Apply CO4

Lab Experiments

1. Draw NMOS characteristics and Determine
   i. Cut-Off Region
   ii. Ohmic or Linear Region
   iii. Saturation Region
2. a. Design an **Inverte**r with given specifications, completing the design flow mentionedbelow: a. Draw the schematic and verify the following
   i. DC Analysis
   ii. Transient Analysis

   b. Draw the Layout and verify the DRC, check for LVS Extract RC and back annotate the same and verify the Design Verify & Optimize for Time, Power andArea to the given constraint

3. a. Draw **CMOS inverter with load capacitance** of 0.1pF and set the widths of inverterwith Wn=Wp, Wn = 2Wp, Wn = Wp/2 and length at selected technology. Carryout the fallowing
   i. Set the input signal to a pulse with rise time, fall time of 1ns and pulse with of10ns and time period of 20ns and plot the input voltage and output voltage of designed inverter.
   ii. From the simulation results compute tpHL, tpLH and td for all three geometricalsettings of width.
   iii. Tabulate the results of delay and find the best geometry for minimum delay forCMOS inverter

   b. Draw layout of inverter with Wp/Wn=40/20, use optimum layout methods. Verify for DRC and LVS, extract parasitic and perform post layout simulations,compare the results.
4. Design of Dynamic CMOS Logic, Y= AB + C
5. Design of Domino CMOS Logic, Y = (A+B) * C
6. Draw the schematic of 2- input CMOS NAND gate having similar delay as that of CMOS inverter computed in experiment 2. Verify the functionality of NAND gate and also find out the delay tdfor all four possible combinations of input vectors. Table the results. Increase the drive strength to 2X and 4X and tabulate the results.
   b. Draw layout of NAND with Wp/Wn=40/20, use optimum layout methods. Verify for DRC and LVS, extract parasitic and perform post layout simulations, compare the results.
7. a. Draw the schematic of Buffer using inverter and verify the simulation.
   b. Draw layout of BUFFER circuit, verify for DRC and LVS, extract parasitic and perform postlayout simulations, compare the results.
8. Draw the schematic of TRI State INVERTER and TRI State Buffer using MOSFETs and verify the simulation. Draw layout and verify for DRC and LVS, extract parasitic and perform post layout simulations, compare the results.
9. a. Draw the schematic of D-latch using inverter and verify the simulation.
   b. Draw layout of D-latch circuit, verify for DRC and LVS, extract parasitic and perform postlayout simulations, compare the results.
10. a. Draw the schematic of D FF using gates and verify the simulation.
    b. Draw Layout of D FF Verify for DRC and LVS, extract parasitic and perform post layout simulations, compare the results.

Course Outcomes: After completing the course, the students will be able to	
23VDE213.1	Analyze issues of On-chip interconnect Modeling and Interconnect delay Calculation
23VDE213.2	Analyze the Switching Characteristics in Digital Integrated Circuits.
23VDE213.3	Use the Dynamic Logic circuits in state-of-the-art VLSI chips.
23VDE213.4	Study critical issues such as ESD protection, Clock distribution, Clockbuffering, and Latch phenomenon
23VDE213.5	Use Bipolar and Bi-CMOS circuits in very high-speed design
23VDE213.6	Apply the concept of Chip I/O's & Design for manufacturability to estimate yield of IC

Reference Books

1. Neil Weste and K. Eshragian, "Principles of CMOS VLSI Design: A System Perspective", Second Edition, Pearson Education (Asia) Pvt. Ltd. 2000.
2. Wayne, Wolf, "Modern VLSI Design: System on Silicon" Prentice Hall PTR/Pearson Education, Second Edition, 1998.
3. Douglas A Pucknell& Kamran Eshragian, "Basic VLSI Design" PHI 3rd Edition (original Edition – 1994).

Text Books

1. Sung Mo Kang &Yosuf Leblebici, "CMOS Digital Integrated Circuits: Analysis andDesign", Tata McGraw-Hill, Third Edition.

Assessment Process

Professional Core with Integrated Lab (PCI) – Course with Lab

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Dept. of Electronics and Communication Engineering
M.Tech (VLSI Design and Embedded Systems)
Choice Based Credit System (CBCS and Outcome Based Education (OBE)

Semester: I

Course Name: Advanced Digital System Design Using VERILOG **Course Code:23VDE214**

L: T: P: J	**2 : 0 :2 :2**	**CIA Marks:** 50
Credits:	**4**	**SEA Marks:** 50
Hours/Week (Total)	**6**	**SEA Duration:** 03 Hours

Pre-Requisites: Understand Boolean algebra and simplification techniques, Basics understanding of combinational and sequential logic circuits, Basics of C language, Knowledge of Mealy and Moore Models and CMOS Circuits.

Course Learning Objectives: The students will be able to

1	Understand basics of HDL Verilog, Design Methodology for digital system, functional verification and Synthesis.
2	Understand Combinational and Sequential circuits using Verilog.
3	Analyze synthesized combinational and sequential circuits
4	Understand Behavioral level modeling and Modelling of Mealy and Moore based circuits
5	Understand System Verilog User defined Data types and Enumerated Data types, Arrays, Structures and Unions

Module-1: Introduction to Digital System	**No. of Hours**	**Blooms cognitive Levels**
ASIC Design Flow, Introduction to Verilog HDL, Language Constructs and Conventions in Verilog HDL, and Gate Level Modeling Study of any Synthesis tools for netlist generation and Design analysis procedure. **Lab Experiment: 1 & 2**	**10**	**Apply CO1**
Module-2 : Combinational Logic Design		
Modeling at Data Flow Level, Continuous Assignment Structures, Delays and Continuous Assignments, Assignment the two Vectors, Operators, Verilog HDL for combinational Circuits, Design of Adder, Subtractor, Decoders, Encoders and Multiplexer, Synthesis of different Verilog combinational designs. **Lab Experiment: 3 & 4**	**10**	**Apply CO2**
Module-3: Sequential Logic Design		
Modeling at Behavioral Level Operator and Assignments, Modeling for Synthesizable RTL, Procedural assignments, Control and looping blocks (IF else, Case, forever, Repeat) Verification constructs (Assertion statements), FSM modeling, Functions, Tasks, Synthesis of Simple IPs and Sequential designs and their design analysis, Mealy and Moore FSMs. **Lab Experiment: 5 & 6**	**10**	**Apply CO3**
Module-4: System Verilog User-Defined and Enumerated Data Types		
User-defined types-Local typedef declarations, External typedef declarations, Naming convention for user-defined types, Enumerated data types: Data type of enumerated type values, Typed and anonymous enumerations, Strong typing on enumerated type operations, Special	**10**	**Apply CO4**

Module-5: SystemVerilog Arrays, structures and Unions		
Structures, Typed and Anonymous structures, Assigning Values to structures, Passing Structures through ports, Unions and Arrays – Packed and Unpacked arrays, Assigning values to arrays, Copying Arrays, Arrays of Arrays, Arrays of Structures and Unions. An example of using arrays using System Verilog. **Lab Experiment: 9 & 10**	**10**	**Apply CO5**

Lab Experiments:

1. Describe 2x1 line multiplexer using universal gates. Realize 8x1 multiplexer using 2x1 as a Component. Write the Verilog code and test it.
2. Design a 4-bit ripple carry adder using RTL coding and verify the design. Verify the design with different delays.
3. Design a 4-bit magnitude comparator using Dataflow modeling in Verilog and test it.
4. Develop a Verilog code for T flip flop, Use T-flip flop as low-level design, to realize 4-bit Asynchronous counter and verify the design.
5. Develop a Mod-16 up-down counter using Mealy/Moore machine. Write the Verilog code and testthe design.
6. Write Verilog code to detect a 3bit sequence (101) using Mealy/Moore model. and verify the Functionality.
7. Develop a System Verilog program for State sequencer using Enumerated data types.
8. Develop System Verilog program to use arrays of structures to model an instruction register.
9. Develop System Verilog program to model structures and packed structures.
10. Develop a System Verilog program to model ALU with Structures and Unions.

Project: Any IP design (UART, I2C) using Verilog HDL and Verification.

Course Outcomes: After completing the course, the students will be able to	
23VDE214.1	Develop Verilog programs using gate level modelling with basic knowledge of VerilogHDL
23VDE214.2	Design and develop Verilog modules for combinational circuits in Verilog HDL
23VDE214.3	Design and develop Verilog modules for Sequential circuits in Verilog HDL
23VDE214.4	Design System Verilog programs using Enumerated data types
23VDE214.5	Design System Verilog programs using structures and arrays.

Reference Books
1. Samir Palnitkar, "**Verilog HDL: A Guide to Digital Design and Sysnthesis"** PearsonEducation, second edition.
2. Stuart Sutherland, Simon Davidmann, Peter Flake, **"System Verilog for Design"**, by Springer Science+Business Media Dordrecht, 2004
3. T.R. Padmanabhan, B. Bala Tripura Sundari**, Design through Verilog HDL,** Wiley Pub 2007.
4. S. Brown & Z. Vransesic, **"Fundamental of digital Logic with Verilog Design",** TMH. 2013

Marks Distribution for Assessment:

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Dept. of Electronics and Communication Engineering M.Tech (VLSI Design and Embedded Systems) Choice Based Credit System (CBCS and Outcome Based Education (OBE)			
Semester: I			
Course Name: Internet of Things and It's Applications		**Course Code: 23VDEP2153**	
L: T: P: J	**3: 0: 2 : 0**	**CIA Marks:** 50	
Credits	**4**	**SEA Marks:** 50	
Hours/Week (Total)	**5**	**SEA Duration:** 03 Hours	
Pre-Requisites: Embedded Systems, Programming in C.			
Course Learning Objectives: The students will be able to			
1	Assess the genesis and impact of IoT applications, architectures in real world		
2	Illustrate diverse methods of deploying smart objects and connect them to network		
3	Compare different Application protocols for IoT		
4	Infer the role of Data Analytics and Security in IoT		
5	Identify sensor technologies for sensing real world entities and understand the role of IoT in various domains of Industry.		

Module-1: Introduction to IoT	**No. of Hours**	**Blooms cognitive Levels**
What is IoT? Genesis of IoT, IoT and Digitization, IoT Impact, Convergence of IT and IoT, IoT Challenges, IoT Network Architecture and Design, Drivers Behind New Network Architectures, Comparing IoT Architectures, A Simplified IoT Architecture, IoT Data Management and Compute Stack	**10**	**Understand CO1**
Module-2: Engineering IoT networks		
Smart Objects: The "Things" in IoT, Sensors, Actuators, and Smart Objects, Sensor Networks, Connecting Smart Objects, Communications Criteria	**10**	**Understand CO2**
Module-3: IP as the IoT Network Layer		
The Business Case for IP, The need for Optimization, Optimizing IP for IoT, Profiles and Compliances, Application Protocols for IoT, The Transport Layer, IoT Application Transport Methods(SCADA only).	**10**	**Understand CO3**
Module-4: Data and Analytics for IoT		
An Introduction to Data Analytics for IoT, Machine Learning, Big Data Analytics Tools and Technology, Edge Streaming Analytics, Network Analytics, Securing IoT, A Brief History of OT Security, Common Challenges in OT Security, How IT and OT Security Practices and Systems Vary, Formal Risk Analysis Structures: OCTAVE and FAIR	**10**	**Understand CO4**
Module-5: IoT Physical Devices and Endpoints		
Arduino UNO: Introduction to Arduino, Arduino UNO, Installing the Software, Fundamentals of Arduino Programming. IoT Physical Devices and Endpoints – Raspberry Pi: Introduction to Raspberry Pi, About the Raspberry Pi Board: Hardware Layout, Operating Systems onRaspberry Pi, Configuring Raspberry Pi, Programming Raspberry Pi withPython, Wireless Temperature Monitoring, Remote access to Raspberry Pi, Smart and Connected Cities, Strategy for Smarter Cities, Smart City IoT Architecture, Smart City Security Architecture, Smart City Use-Case Examples.	**10**	**Apply CO5**

Lab Experiments
1. Arduino Basics - Understanding Arduino Uno Board and Components, Installing and work with Arduino IDE, Fundamentals of Arduino Programming.

3. Program to display a message on LCD using Arduino. Specify the position and display a character. Display Special symbols such as Smiley, bouncing ball, scrolling message, display the status of a pushbutton ON/OFF
4. Program to control LED interfaced to Arduino using Bluetooth (HC-05)
5. Program to control speed of a dc motor using Pulse Width Modulation.
6. Configuring Raspberry Pi, OS installation. Blink an LED using Raspberry Pi.
7. Interface an IR sensor to detect the presence of a person using Raspberry Pi.
8. Interface an Ultrasonic sensor to Raspberry Pi to measure the distance of object
9. Interface DHT 11 sensor to using Raspberry Pi to measure the ambient temperature. Demonstrate wireless up-dation of the measured temperature in cloud.
10. Demonstrate Remote access to Raspberry Pi.
11. Revision
12. Test

Course Outcomes: After completing the course, the students will be able to	
23VDEP2153.1	Interpret the impact and challenges posed by IoT networks leading to new architectural models.
23VDEP2153.2	Compare and contrast the deployment of smart objects and the technologies to connect them to network.
23VDEP2153.3	Appraise the role of IoT protocols for efficient network communication.
23VDEP2153.4	Elaborate the need for Data Analytics and Security in IoT.
23VDEP2153.5	Illustrate different sensor technologies for sensing real world entities and identify the applications of IoT in Industry.

Reference Books

1. David Hanes, Gonzalo Salgueiro, Patrick Grossetete, Robert Barton, Jerome Henry,"IoT Fundamentals: Networking Technologies, Protocols, and Use Cases for the Internet of Things", 1st Edition, Pearson Education (Cisco Press Indian Reprint). (ISBN: 978-9386873743)
2. Vijay Madisetti and Arshdeep Bahga, "Internet of Things (A Hands-on-Approach)", 1st Edition, VPT, 2014. (ISBN: 978-8173719547)
3. Raj Kamal, "Internet of Things: Architecture and Design Principles", 1st Edition, McGraw Hill Education, 2017. (ISBN: 978-9352605224

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Dept. of Electronics and Communication Engineering
M.Tech (VLSI Design and Embedded Systems)
Choice Based Credit System (CBCS and Outcome Based Education (OBE)

Semester: I

RESEARCH METHODOLOGY AND IPR **course code: 23VDE216**

L: T :P: J: 0	**2: 0 : 0 : 0**	**CIA Marks:** 50
Credits	**2**	**SEA Marks:** 50
Hours/Week (Total)	**2**	**SEA Duration:** 03 Hours

Pre-Requisites: Use of internet and online database, clarity on research question/problem and basic of statistics

Course Learning Objectives: The students will be able to

1	To give an overview of the research methodology and explain the technique of defining a research problem
2	To explain the functions of literature review, carry out literature search and develop conceptual frameworks
3	To explain various experimental designs in research and data handling like data sampling and data collection methods
4	To interpret the research findings and prepare a research report
5	To build awareness on the various forms of IPR and to build the perspectives on the concepts and to develop the linkages in technology innovation and IPR.

Module-1: Introduction to Research Methodology	**No. of Hours**	**Blooms Cognitive Levels**
Research Methodology: Introduction, Meaning of Research, Objectives of Research, Motivation in Research, Types of Research, Research Approaches, Significance of Research, Research Methods versus Methodology, Research and Scientific Method, Importance of Knowing How Research is Done, Research Process, Criteria of Good Research **Defining the Research Problem**: Research Problem, Selecting the Problem, Necessity of Defining the Problem, Technique Involved in Defining a Problem, An Illustration Problems Encountered by Researchers in India.	**05**	**Understand CO1**
Module-2: Literature Review		
Reviewing the literature: Place of the literature review inresearch, Bringing clarity and focus to your research problem, Improving research methodology, Broadening knowledge base in research area, enabling contextual findings, How to review the literature, searching the existing literature, reviewing the selected literature, developing a theoretical framework, Developing a conceptual framework, writing about the literature reviewed. **Research Design**: Meaning of Research Design, Need for Research Design, Features of a Good Design, Important Concepts Relating to Research Design, Different Research Designs, Basic Principles of Experimental Designs, Important ExperimentalDesigns. Use of Endnote or mendeley	**05**	**Apply CO2**
Module-3: Data Sampling and Testing of Hypothesis		

Design of Sampling: Introduction, Sample Design, Sampling andNon-sampling Errors, Sample Survey versus Census Survey, Types of Sampling Designs. **Measurement and Scaling**: Qualitative and Quantitative Data, Classifications of Measurement Scales, Goodness of Measurement Scales, Sources of Error in Measurement Tools, Scaling, Scale Classification Bases, Scaling Technics, Multidimensional Scaling, Deciding the Scale. **Data Collection:** Experimental and Surveys, Collection of Primary Data, Collection of Secondary Data, Selection of Appropriate Method for Data Collection. **Testing of Hypotheses**: Hypothesis, Basic Concepts Concerning Testing of Hypotheses, Testing of Hypothesis, Test Statistics and Critical Region, Critical Value and Decision Rule, Procedure for Hypothesis Testing, Hypothesis Testing for Mean, Proportion, Variance, for Difference of Two Mean, for Difference of Two Proportions, for Difference of Two Variances, P-Value approach, Power of Test, Limitations of the Tests of Hypothesis.Case Study Method, ANOVA test using excel or similar tools.	**05**	**Apply CO3**
Module-4: Interpretation and Report Writing		
Interpretation: Meaning of Interpretation, Technique of Interpretation, Precaution in Interpretation. **Report Writing:** Significance of Report Writing, Different Steps in Writing Report, Layout of the Research Report, Types of Reports, Oral Presentation, Mechanics of Writing a Research Report, Precautions for Writing Research Reports. Introduction to Latex and various templates for report and paper writing. Research paper writing using Latex	**05**	**Analyze CO4**
Module-5: Intellectual Property Rights		
Intellectual Property: The Concept, Intellectual Property System in India, Development of TRIPS Complied, Regime in India, Patents Act, 1970, Trade Mark Act, 1999, The Designs Act, 2000, The Geographical Indications of Goods (Registration and Protection) Act1999, Copyright Act,1957, The Protection of Plant Varieties and Farmers' Rights Act, 2001, The Semi-Conductor Integrated Circuits Layout Design Act, 2000, Trade Secrets, Utility Models, IPR and Biodiversity, The Convention on Biological Diversity (CBD) 1992, Competing Rationales for Protection of IPRs, Leading International Instruments ConcerningIPR, World Intellectual Property, Organisation (WIPO), WIPO and WTO, Paris Convention for the Protection of Industrial Property, National Treatment, Right ofPriority, Common Rules, Patents, Marks, Industrial Designs,Trade Names, Indications of Source, Unfair Competition Introduction to Patents and Copyrights. Case study on company IPR	**05**	**Understand CO5**

Course Outcomes: After completing the course, the students will be able to	
23VDE216.1	Understand and define research problem
23VDE216.2	Explain and carry out literature review based on the research problem
23VDE216.3	Apply sampling and data collection techniques and carry out parametric tests of Hypothesis for the research problem
23VDE216.4	Interpret the research findings and create a report
23VDE216.5	Explain various forms of IPR and develop the linkages in technology

Reference Books
1. Trochim, "Research Methods: the concise knowledge base", Atomic Dog Publishing 2005. 2. Fink A, "Conducting Research Literature Reviews: From the Internet to Paper", Sage Publications 2009. 3. C.R. Kothari, Gaurav Garg, "Research Methodology: Methods and Techniques", New Age International 4 th Edition, 2018. 4. Ranjit Kumar, "Research Methodology a step-by-step guide for beginners" (For the topic Reviewing the literature under module 2), SAGE Publications 3 rd Edition, 2011. 5. Firuza Karmali (Aibara), " A Short Introduction to LaTeX: A Book for Beginners", Create space Independent Publishing Platform, 2019.

Marks Distribution for Assessment:

<table>
<tr><th rowspan="2">PCC</th><th rowspan="2">CIA</th><th rowspan="2">SEA</th><th colspan="3">CIA (50)</th><th rowspan="2">SEA
Conduction: 100 M
Reduced to: 50 M</th></tr>
<tr><th></th><th>I</th><th>II</th></tr>
<tr><td rowspan="5">Conduction</td><td rowspan="5">50</td><td rowspan="5">50</td><td rowspan="2">Written Test</td><td>50</td><td>50</td><td rowspan="4">Five questions with each of 20 marks (with internal choice). Student should answer one full question from each module</td></tr>
<tr><td colspan="2">Average of two tests – 25 Marks</td></tr>
<tr><td>Assignment</td><td colspan="2">15</td></tr>
<tr><td>AAT</td><td colspan="2">10</td></tr>
<tr><td colspan="3">Total – 50 marks</td><td>Total – 50 marks</td></tr>
</table>

Dept. of Electronics and Communication Engineering
M.Tech (VLSI Design and Embedded Systems)
Choice Based Credit System (CBCS and Outcome Based Education (OBE)

Semester: II

Course Name: VLSI Testing and Testability		**Course Code: 23VDE221**
L: T: P: J:	**4: 0: 0: 0**	**CIE Marks: 50**
Credits:	**4**	**SEE Marks: 50**
Hours/Week:	**4 (50)**	**SEE Duration: 03 Hours**

Pre-Requisites: Basic courses on Digital circuit design, Knowledge about simulation and Logic Design.

Course Learning Objectives: The students will be able to

1	Learn various types of faults and fault modelling
2	Comprehend the need for testing and testable design of digital circuits
3	Illustrate methods and algorithms for testing digital combinatorial networks and test pattern generation
4	Exemplify methods for testing sequential circuits and memory testing
5	Inferring testing methods using Boundary scan, Built-in self-test and other advanced topics in digital circuit design

Module-1: Introduction, VLSI Testing Process and Fault Models	**No. of Hours**	**Blooms Cognitive Levels**
Testing Philosophy, Role of Testing, Digital and Analog VLSI Testing, VLSI Technology Trends affecting Testing, Types of Testing, Fault Modelling: Defects, Errors and Faults, Functional Versus Structural Testing, Levels of Fault Models, Single Stuck-at Fault.	**10**	**Understand CO1**
Module-2: Logic and Fault Simulation		
Simulation for Design Verification and Test Evaluation, Modelling Circuits for Simulation, Algorithms for True-value Simulation, Algorithms for Fault Simulation, ATPG. Fault Diagnosis of Digital Circuits, Test Generation Techniques for Combinational Circuits, Detection of Multiple Faults in Combinational Logic Circuits.	**10**	**Apply CO2**
Module-3: Testability Measures		
SCOAP Controllability and Observability, High Level Testability Measures, Digital DFT and Scan Design: Ad- Hoc DFT Methods, Scan Design, Partial-Scan Design, Variations of Scan, Ad-Hoc DFT Methods.	**10**	**Apply CO3**
Module-4: Built-In Self-Test		
The Economic Case for BIST, Random Logic BIST: Definitions, BIST Process, Pattern Generation, Response Compaction, Built-In Logic Block Observers, Test-Per-Clock, Test-Per Scan BIST Systems, Circular Self-Test Path System, Memory BIST, Delay Fault BIST, Logic Built in Self-Test.	**10**	**Apply CO4**
Module-5: Boundary Scan Standard		
Motivation, System Configuration with BoundaryScan: TAP Controller and Port, Boundary Scan Test Instructions, Pin Constraints of the Standard, Boundary Scan Description Language: BDSLDescription Components, Pin Descriptions, Boundary Scan for Asynchronous Processor	**10**	**Apply CO5**

Reference Books
1. Essentials of Electronic Testing for Digital, Memory and Mixed Signal VLSI Circuits -M.L.Bushnell, V. D. Agrawal, Kluwer Academic Publishers. 2. Digital Systems and Testable Design - M. Abramovici, M.A.Breuer and A.D Friedman,Jaico Publishing House 3. Digital Circuits Testing and Testability - P.K. Lala, Academic Press

<table>
<tr><th rowspan="2">PCC</th><th rowspan="2">CIA</th><th rowspan="2">SEA</th><th colspan="3">CIA (50)</th><th rowspan="2">SEA
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<tr><td>Assignment</td><td colspan="2">15</td></tr>
<tr><td>AAT</td><td colspan="2">10</td></tr>
<tr><td colspan="3">Total – 50 marks</td><td>Total – 50 marks</td></tr>
</table>

i) CIA: 50%

IA Test: 2 IA tests - Each of 50 Marks	Average of 2 tests – scaled down to 25 M
Assignment – Two assignments – one for 10 marks and another for 5 marks	15 Marks
Additional Assessment Tools (AAT) – Oral /Online Quizzes, Presentations, Group discussions, Case studies, Term Paper, Open ended experiments, Mini industrial/social/rural Projects, Two-minute video on latest topic, Short MOOC courses, Practical Orientation on Design thinking, creativity & Innovation, Participatory & Industry integrated learning, Practical activities, Problem solving exercises, Participation in seminars/academic events/symposia and any other activity	10 Marks
Total	**50 Marks**

ii) SEA: 50%

Theory Exam	5 questions to answer each of 20 Marks 2 questions from each module with internal choice Student should answer one full question from each module	20 M x 5 = **100 M** **reduced to 50 M**
	Total	**50 Marks**

Dept. of Electronics and Communication Engineering
M.Tech (VLSI Design and Embedded Systems)
Choice Based Credit System (CBCS and Outcome Based Education (OBE))

Semester: II

Course Name: Low Power VLSI Design		**Course Code: 23VDE222**
L: T: P: J	**3: 0 :2: 0**	**CIA Marks:** 50
Credits:	**4**	**SEA Marks:** 50
Hours/Week (Total)	**5**	**SEA Duration:** 03 Hours

Pre-Requisites: CMOS Logic Design, Power and energy relations in a capacitor, MOSFET Characteristics, Short channel effects in a MOSFET, Combinational and Sequential circuits.

Course Learning Objectives: The students will be able to

1	Understand the state-of-the-art approaches to power estimation and reduction.
2	Describe the various power reduction and the power estimation methods.
3	Explain power dissipation at all layers of design hierarchy from technology, circuit, logic, architecture and system.
4	Practice the low power techniques using current generation design style and process technology.
5	Understand the advanced techniques in low power design methods.

Module-1: Introduction to Low power Design	**No. of Hours**	**Blooms Cognitive Levels**
Introduction: Need for low power VLSI chips, charging and discharging capacitance, short circuit current in CMOS leakage current, static current, basic principles of low power design, low power figure of merits. **Simulation power analysis**: SPICE circuit simulation, discrete transistor modeling and analysis, gate level logic simulation, architecture level analysis, data correlation analysis in DSP systems, Monte Carlo simulation.	**10**	**Apply CO1**
Module-2: Power Estimation methods		
Probabilistic power analysis: Random logic signals, probability & frequency, probabilistic power analysis techniques, signal entropy. **Circuit**: Transistor and gate sizing, equivalent pin ordering, network restructuring and reorganization, special latches and flip flops, low power digital cell library, adjustable device threshold voltage.	**10**	**Apply CO2**
Module-3: Low power Design at Logic Level and Clock distribution		
Logic: Gate reorganization, signal gating, logic encoding, state machine encoding, pre-computation logic. **Low power Clock Distribution:** Power dissipation in clock distribution, single driver Vs distributed buffers, Zero skew Vs tolerable skew, chip & package co design of clock network.	**10**	**Apply CO3**
Module-4: Low power Design at Architecture/System Level		
Low power Architecture & Systems: Power & performance management, switching activity reduction, parallel architecture with voltage reduction, flow graph transformation. **Low power arithmetic components**: Introduction, circuit design style, adders, multipliers, division.	**10**	**Analyze CO4**
Module-5: Low power Memory Design and Algorithm level methods		
Low power memory design: Introduction, sources and reductions of power dissipation in memory subsystem, sources of power dissipation in DRAM and SRAM. **Algorithm & Architectural Level Methodologies**: Introduction, design flow, Algorithmic level analysis & optimization, Architectural level estimation & synthesis.	**10**	**Analyze CO5**

List of Experiments:

1. Design a traditional CMOS inverter schematic with 45 nm technology and plot its transfer (DC) characteristics and transient characteristics. Also, design a SC-SS (Low power) CMOS inverter schematic with 45 nm technology and plot its transfer (DC) characteristics and transient characteristics. Tabulate the readings (Delay, Power consumption, Power-Delay Product) for both the schematics and plot a comparison graph.

2. Design a traditional 2-input CMOS NAND gate schematic with 45 nm technology and plot its transfer (DC) characteristics and transient characteristics. Also, design a SC-SS (Low power) 2-input CMOS NAND gate schematic with 45 nm technology and plot its transfer (DC) characteristics and transient characteristics. Tabulate the readings (Delay, Power consumption, Power-Delay Product) for both the schematics and plot a comparison graph.

3. Design a traditional 2-input XOR gate (12T) schematics with 45 nm technology and plot its transfer (DC) characteristics and transient characteristics. Also, design a SC-SS (Low power) 2-input CMOS XOR gate schematic with 45 nm technology and plot its transfer (DC) characteristics and transient characteristics. Tabulate the readings (Delay, Power consumption, Power-Delay Product) for both the schematics and plot a comparison graph.

4. Design a traditional Half Adder schematic with 45 nm technology and plot its transient response. Also, design a SC-SS (Low power) Half Adder schematic with 45 nm technology and plot its transient response. Tabulate the readings (Delay, Power consumption, Power-Delay Product) for both the schematics and plot a comparison graph.

5. Design a traditional Full Adder schematic with 45 nm technology and plot its transient response. Also, design a SC-SS (Low power) Full Adder schematic with 45 nm technology and plot its transient response. Tabulate the readings (Delay, Power consumption, Power-Delay Product) for both the schematics and plot a comparison graph.

6. Design a traditional D Flip-Flop schematic with 45 nm technology and plot its transient response. Also, design a D Flip-Flop with self clock-gating schematic (Low power) with 45 nm technology and plot its transient response. Tabulate the readings (Delay, Power consumption, Power-Delay Product) for both the schematics and plot a comparison graph.

7. Design a 4-bit ripple carry adder schematic with 45 nm technology and plot its transient response. Also, design a 4-bit Carry save adder schematic with 45 nm technology and plot its transient response. Tabulate the readings (Delay, Power consumption, Power-Delay Product) for both the schematics and plot a comparison graph.

8. Design a basic 6T SRAM Cell schematic with 45 nm technology and plot its transient response. Also, design a 10T SRAM Cell schematic with 45 nm technology and plot plot its transient response. Tabulate the readings (Delay, Power consumption) for both the schematics and plot a comparison graph.

EDA Tools: Cadence-Virtuoso, LT Spice.

Course Outcomes: After completing the course, the students will be able to	
23VDE222.1	Identify the sources of power dissipation in CMOS circuits.
23VDE222.2	Perform power analysis using simulation-based approaches and probabilistic analysis.
	Develop the optimization and trade-off techniques that involve power dissipation of

23VDE222.4	Apply the low power design techniques at the architecture and system level.
23VDE222.5	Analyze and optimize the low power memory design techniques and algorithm level methods.
23VDE222.6	Develop the practical design techniques and their analysis at various levels of design abstraction and analyze how these are being captured in the latest design automation environments.

Reference Books

1. Practical Low Power Digital VLSI Design, Gary K. Yeap, Kluwer Academic Publishers, ISBN 978-1- 4613-7778-8, 2002.
2. Low Power Design Methodologies, Jan M. Rabaey and Massoud Pedram, Kluwer Academic Publishers, 5th reprint, 2010.
3. Low-Power CMOS VLSI Circuit Design Kaushik Roy and Sharat Prasad, John Wiley, 2000.
4. Low power digital CMOS design A. P. Chandrasekaran and W. Broadersen Kluwer academic,1995.
5. Low-Power VLSI Circuits and Systems, Ajit Pal, Springer publications, 2015.

Marks Distribution for Assessment:

<table>
<tr><th rowspan="2">PCI</th><th rowspan="2">CIA</th><th rowspan="2">SEA</th><th colspan="3">CIA (50)</th><th rowspan="2">SEA
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<tr><td rowspan="4">Conduction</td><td rowspan="4">50</td><td rowspan="4">50</td><td rowspan="2">Written Test</td><td>50</td><td>50</td><td rowspan="4">Five questions with each of 20 marks (with internal choice). Student should answer one full question from each module</td></tr>
<tr><td colspan="2">Average of two tests – 50 marks scaled down to 15 marks</td></tr>
<tr><td>Assignment</td><td colspan="2">Average of 2 Assignments – 10M</td></tr>
<tr><td>Practical</td><td colspan="2">Weekly Assessment – 10 Marks
IA test – 15 Marks
(IA test to be conducted for 50 M and scaled down to 15M)</td></tr>
<tr><td></td><td></td><td></td><td colspan="3">Total – 50 Marks</td><td>Total – 50 Marks</td></tr>
</table>

i) CIA: 50%

Theory	**IA Test** (Theory): 2 IA tests - each of 50 Marks – Average of 2 tests scaled down to 15 Marks **Assignment**: 2 Assignments – each of 10 marks	25 Marks
Lab	**Weekly Assessment** – 10 Marks **Practical test (1)** - 15 marks	25 Marks
	Total	**50 Marks**

ii) SEA: 50%

Question Paper:

Theory Exam	5 questions to answer, each of 20 Marks 2 questions from each module with internal choice Student should answer one full question from each module	20 M x 5 = **100 M** **Reduced to 50 M**

Dept. of Electronics and Communication Engineering
M.Tech (VLSI Design and Embedded Systems)
Choice Based Credit System (CBCS and Outcome Based Education (OBE)

Semester: II

Course Name: DESIGN OF ANALOG AND MIXED MODE VLSI CIRCUITS
Course Code: 23VDE223

L: T: P: J	**3 : 0 : 2 : 0**	**CIA Marks:** 50
Credits:	**4**	**SEA Marks:** 50
Hours/Week (Total)	**5(50)**	**SEA Duration:** 03 Hours

Pre-Requisites: General considerations of MOS devices, MOS I/V Characteristics, second order effects, Basics to Amplifiers, Introduction to concepts of current mirrors and Op-Amp,Op-amp Parameters and Introduction to DAC and ADC.

Course Learning Objectives: The students will be able to

1	Describe the basic physics and operation of MOS devices
2	Exemplify single-stage and differential amplifiers and current mirrors
3	Describe operational amplifiers
4	Learn the design of phase-locked-loops
5	Know the role of Data converters in an ever-increasing digital world.

Module-1: Single stage Amplifier	**No. of Hours**	**Blooms Cognitive Levels**
Single stage Amplifier: Common Source stage, Source follower, Common-gate stage, Cascode Stage. Lab Experiment: 1 to 5	**10**	**Understand CO1**
Module-2: Differential Amplifiers		
Differential Amplifiers: Single ended and differential operation, Basic differential pair, Common mode response, Differential pair with MOS loads, Gilbert cell. Lab Experiment: 6 & 7	**10**	**Apply CO2**
Module-3: Passive and Active Current Mirrors & Operational Amplifiers (Part-1)		
Passive and Active Current Mirrors: Basic current mirrors, Cascode Current mirrors, Active Current mirrors. **Operational Amplifiers (part-1):** General Considerations, OneStage OP-Amp, Two Stage OP-Amp, Gain boosting Lab Experiment: 8	**10**	**Apply CO3**
Module-4: Operational Amplifiers (part-2) & Phase Locked Loops:		
Operational Amplifiers (part-2): Common Mode Feedback, Slew rate, Power Supply Rejection. Phase Locked Loops: Simple PLL, Charge pump PLLs, Non-ideal effects in PLLs, Delay-Locked Loops.	**10**	**Apply CO4**
Module-5: Data Converter Architectures:		
Data Converter Architectures: DAC & ADC Specifications, Current Steering DAC, Charge Scaling DAC, Cyclic DAC, Pipeline DAC. Flash ADC, Pipeline ADC, Integrating ADC	**10**	**Understand CO5**

Lab Experiments:

1. Design the Common Source amplifier with Current Source Load completing the design flow for
   a. Draw the schematic and verify the following
      - DC Analysis
      - AC Analysis
      - Transient Analysis

   b. Draw the Layout and verify the DRC, check for LVS, Extract RC and back annotate the same and verify the Design.
2. Design the Common Source amplifier with Diode connected load completing the design

- DC Analysis
- AC Analysis
- Transient Analysis

b. Draw the Layout and verify the DRC, check for LVS, Extract RC and back annotate the same and verify the Design.

3. Design the Common Source **amplifier with resistive load** completing the design flow for
   a. Draw the schematic and verify the following
      - DC Analysis
      - AC Analysis
      - Transient Analysis

   b. Draw the Layout and verify the DRC, check for LVS d. Extract RC and back annotate the same and verify the Design.
4. Design the **Common Drain** with given specifications completing the design flow for
   a. Draw the schematic and verify the following
      - DC Analysis
      - AC Analysis
      - Transient Analysis

   b. Draw the Layout and verify the DRC, check for LVS d. Extract RC and back annotate the same and verify the Design.
5. Design the **Common Gate** with given specifications completing the design flow for
   a. Draw the schematic and verify the following
      - DC Analysis
      - AC Analysis
      - Transient Analysis

   b. Draw the Layout and verify the DRC, check for LVS, Extract RC and back annotate the same and verify the Design.
6. Design the **Current Mirror** with given specifications completing the design flow for
   a. Draw the schematic and verify the following
      - DC Analysis
      - AC Analysis
      - Transient Analysis

   b. Draw the Layout and verify the DRC. Check for LVS, Extract RC and back annotate the same and verify the Design.
7. Design the **Differential Amplifier** completing the design flow for
   a. Draw the schematic and verify the following
      - DC Analysis
      - AC Analysis
      - Transient Analysis

   b. Draw the Layout and verify the DRC. Check for LVS, Extract RC and back annotate the same and verify the Design.
8. Design an **op-amp** using the **differential amplifier** with Common source and Common Drain amplifier in library, completing the design flow mentioned below:
   a. Draw the schematic and verify the following
      - DC Analysis
      - AC Analysis
      - Transient Analysis.

   b. Draw the Layout and verify the DRC, Check for LVS, Extract RC and back annotate the same and verify the Design.

Course Outcomes: After completing the course, the students will be able to	
23VDE223.1	Derive small signal model of MOSFET with second order effects and estimate the parameters for single stage CS, CG, source follower and cascade stage.
23VDE223.2	Design high-performance, stable operational amplifiers with the tradeoffs between speed, precision and power dissipation, study the behaviour of phase-locked-loopsfor the applications.
23VDE223.3	Identify the critical parameters that affect the analog and mixed-signal VLSI circuits' performance.
23VDE223.4	Perform calculations in the digital or discrete time domain, more sophisticated data converters to translate the digital data to and from inherently analog world.
23VDE223.5	Apply concepts of both Analog and digital design for VLSI Technology.
23VDE223.6	Use efficient analytical tools for quantifying the behaviour of basic circuits byinspection.

Reference Books

1. Design of Analog CMOS Integrated Circuits Behzad Razavi TMH 2007
2. CMOS Circuit Design, Layout, and Simulation R. Jacob Baker Wiley Second Edition
3. CMOS Analog Circuit Design Phillip E. Allen, Douglas R. Holberg Oxford UniversityPress Second Edition.

PCI	CIA	SEA	CIA (50)			SEA
				I	II	**Conduction: 100 M Reduced to: 50 M**
Conduction	50	50	Written Test	50	50	Five questions with each of 20 marks (with internal choice). Student should answer one full question from each module
				Average of two tests – 50 marks scaled down to 15 marks		
			Assignment	Average of 2 Assignments – 10M		
			Practical	Weekly Assessment – 10 Marks IA test – 15 Marks (IA test to be conducted for 50 M and scaled down to 15M)		
				Total – 50 Marks		**Total – 50 Marks**

i) CIA: 50%

Theory	**IA Test** (Theory): 2 IA tests - each of 50 Marks – Average of 2 tests scaled down to 15 Marks **Assignment**: 2 Assignments – each of 10 marks	25 Marks
Lab	**Weekly Assessment –** 10 Marks **Practical test (1) -** 15 marks	25 Marks
	Total	**50 Marks**

ii) SEA: 50%

Question Paper:

Theory Exam	5 questions to answer, each of 20 Marks 2 questions from each module with internal choice Student should answer one full question from each module	20 M x 5 = **100 M** **Reduced to 50 M**
		Total **50 Marks**

Dept. of Electronics and Communication Engineering
M.Tech (VLSI Design and Embedded Systems)
Choice Based Credit System (CBCS and Outcome Based Education (OBE)

Semester: II

Course Name: System Verilog for Verification **Course Code: 23VDE224**

L: T: P: J	**2: 0: 2: 2**	**CIA Marks:** 50
Credits:	**4**	**SEA Marks:** 50
Hours/Week (Total)	**6(50)**	**SEA Duration:** 03 Hours

Pre-Requisites: Basics understanding of combinational and sequential logic circuits, Basics of C and C++ language, Knowledge about Simulation, Verilog HDL concepts and programming

Course Learning Objectives: The students will be able to

1	Understand digital system verification using object oriented methods.
2	Learn the System Verilog language for digital system verification.
3	Create/build test benches for the basic design/methodology.
4	Use constrained random tests for verification.
5	Understand concepts of Interprocess communication and functional coverage.

Module-1: Verification Guidelines & Procedural Statements and Routines	**No. of Hours**	**Blooms Cognitive Levels**
Verification Guidelines: The verification process, basic test bench functionality, directed testing, methodology basics, constrained random stimulus, randomization, functional coverage, test bench components,layered testbench. **Connecting the test bench and design** Separating the test bench and design, The interface construct, Stimulus timing, Interface driving and sampling, System Verilog assertions. **Lab Experiment: 1 & 2**	**10**	**Apply CO1**
Module-2: Basic OOP		
Introduction, Think of Nouns, not Verbs, Your First Class, Where to Define a Class, OOP Terminology, Creating New Objects, Object Deallocation, Using Objects, Static Variables vs. Global Variables, Class Methods, Defining Methods Outside of the Class, Scoping Rules, Understanding Dynamic Objects, Public vs. Local , Building a Testbench **Lab Experiment: 3**	**10**	**Apply CO2**
Module-3: Randomization		
Introduction, Randomization in System Verilog, Constraint details, Solution probabilities, Valid constraints, In-line constraints, Random number functions, Common randomization problems, Random control, Random Number Generators. **Lab Experiment: 4 & 5**	**10**	**Apply CO3**
Module-4: Threads and Interprocess Communication		
Working with Threads, Disabling Threads, Events, Semaphores, Mailboxes **Lab Experiment: 6, 7 & 8**	**10**	**Apply CO4**
Module-5: Functional Coverage		
Coverage types, Coverage strategies, Simple coverage example, Anatomy of Cover group and Triggering a Cover group, Data sampling, Cross coverage, Generic Cover groups, Coverage options, Analyzing coverage data, measuring coverage statistics during simulation. **Lab Experiment: 9 & 10**	**10**	**Apply CO5**

Lab Experiments:

1. Develop a System Verilog code to demonstrate two-state and four-state data types.
2. Develop a System Verilog code to demonstrate push_front, pop_front, with respect to Queues.
3. Demonstrate Full adder using System Verilog with 'Interface' construct.
4. Develop a System Verilog code to demonstrate classes.
5. Write a program to create an array (Fixed Array and Dynamic Array) of objects in System Verilog

8. Demonstrate Interprocess Communication in System Verilog.
9. Demonstrate 4-bit adder with the verification environment
10. Write a System Verilog code to declare explicit Bins.

Projects:

1. Verification of Vedic Multiplier using System Verilog.
2. Verification of Convolutional Encoder and Viterbi Decoder using System Verilog.
3. Verification of Signed integer divider using System Verilog.
4. Verification of Wallace Tree Multiplier using System Verilog.
5. Verification of Fixed Point Arithmetic Operations using System Verilog.

Course Outcomes: After completing the course, the students will be able to	
23VDE224.1	Understand the verification guideline in test benches for moderately complex digital circuits.
23VDE224.2	Demonstrate the skill on writing test-benches for design digital systems and connecting them with the design.
23VDE224.3	Apply OOPs concepts to verify and analyze the complete system.
23VDE224.4	Apply constrained random tests benches using System Verilog
23VDE224.5	Demonstrate Threads and Interprocess communication in System Verilog.
23VDE224.6	Apply functional coverage strategies for analyzing coverage of data and coverage statistics.

Reference Books

1. Chris Spear, 'System Verilog for Verification – A guide to learning the Test bench language features', Springer Publications, 2nd Edition, 2010.
2. Stuart Sutherland, Simon Davidmann, Peter Flake, "System Verilog for DesignA guide to using system verilog for Hardware design and modeling", Springer Pulications, 2nd Edition, 2006.
3. Stuart Sutherland, Simon Davidmann, Peter Flake, "System Verilog for Design Second Edition: A Guide to Using System Verilog for Hardware Design and Modeling", Springer Science & Business Media, 15-Sep-2006.
4. Janick Bergeron, "Writing Testbenches Using SystemVerilog", 1st Edition, Springer Publications, 2006.
5. Janick Bergeron, Eduard Cerny, Alan Hunter, and Andy Nightingale, "Verification Methodology Manual for SystemVerilog", Springer Pulications, 2006.

<table>
<tr><th>PBL</th><th>CIA</th><th>SEA</th><th colspan="3">CIA (50)</th><th>SEA
Conduction: 100 M
Reduced to: 50 M</th></tr>
<tr><td rowspan="5">Conduction</td><td rowspan="5">50</td><td rowspan="5">50</td><td rowspan="3">Theory</td><td>I IA</td><td>II IA</td><td rowspan="5">Project
Assessed for 100 marks
reduced to 50 Marks</td></tr>
<tr><td>25</td><td>25</td></tr>
<tr><td colspan="2">Average of 2 tests – 25 M</td></tr>
<tr><td>Practical</td><td colspan="2">Weekly Assessment (Record/Project) – 10 Marks
Lab IA test – 15 Marks</td></tr>
<tr><td colspan="3">Total – 50 Marks</td><td>Total – 50 Marks</td></tr>
</table>

i) CIA: 50%

Theory - 2 IA tests - Each of 25 Marks	25 Marks
Practical **Weekly Assessment -** Lab record/Project – 10 Marks **Lab IA test** – 15 Marks	25 Marks
Total	**50 Marks**

ii) SEA : 50%

Project	Write up – 10 Marks Project report – 25 Marks Presentation & Demonstration - 50 Marks Viva-Voce – 15 Marks	100 Marks Reduced to 50 Marks

B N M Institute of Technology

Dept. of Electronics and Communication Engineering
M. Tech (VLSI Design and Embedded Systems)
Choice Based Credit System (CBCS and Outcome Based Education (OBE)
Semester: II

Course Name: Wearable Technology		**Course Code: 23VDEP2253**
L: T: P: J	**3: 0: 0 :0**	**CIE Marks: 50**
Credits:	**3**	**SEE Marks: 50**
Hours/Week	**3**	**SEE Duration: 03 Hours**

Pre-Requisites: Embedded Systems and Sensors

Course Learning Objectives: The students will be able to

1	To provide a brief overview of the wearable technology, need for development of wearable devices, and its impact on social life.
2	Discuss the applications of various wearable inertial sensors for biomedical applications.
3	Discuss the design and development of various wearable sensors and monitoring devices for use in healthcare applications.
4	Familiar with various wearable locomotive sensors as assistive devices for tracking and navigation.
5	To understand biochemical sensors for wearables and their applications.

Module-1: Wearables: Fundamentals, advancements, and a roadmap for the future	**No. of Hours**	**Blooms cognitive Levels**
World of Wearables, Role of Wearables, Data-information-knowledge-value paradigm, The ecosystem enabling digital life, Attributes of wearables, Taxonomy for wearables, Advancements in wearables, Textiles and clothing: The meta-wearable, Challenges and opportunities, The future of wearables: Defining the research roadmap.	**8**	**Understand CO1**
Module-2: Wearable Sensors and its Applications		
Wearable Inertial Sensors - Accelerometers, Gyroscopic sensors and Magnetic sensors; Ground Force Sensors and Insole Sensors, In-Shoe Force and Pressure Measurement, Force Sensor for Sleep Condition and Respiration on the Bed, Modality of Measurement- Wearable Inertial Sensors, Invisible Sensors, Applications: Fall Risk Assessment, Fall Detection and Gait Analysis, Physical Activity monitoring: Human Kinetics, Cardiac Activity, Energy Expenditure measurement: Pedometers, Actigraphs, Recovery	**8**	**Understand CO2**
Module-3: Medical Applications of Wearable Technologies		
Wearable ECG devices: Basics of ECG and its design, Electrodes and the Electrode–Skin Interface; Wearable EEG devices: Principle and origin of EEG, Basic Measurement set-up, electrodes and instrumentation; Wearable EMG devices: EMG/ SEMG Signals, EMG Measurement – wearable surface electrodes, SEMG Signal Conditioning, Applications.	**8**	**Apply CO3**
Module-4: Wearable Assistive Devices for the Blind and Flexible Sensors		

Wearable Assistive Devices for the Blind - Hearing and Touch sensation, Assistive Devices for Fingers and Hands, Assistive Devices for wrist, forearm and feet, vests and belts, head-mounted devices. Inkjet-Printed Sensors on Flexible Substrates: Introduction, Required Physical Properties of the Printable Ink, Materials for Printed Sensors, Conducting Materials, Semiconducting Materials, Dielectric Materials, Substrates for Flexible Sensors, Polymer-Based Substrates, Paper-Based Substrates, Textile-Based Substrates, Adhesion of Printable Ink with Substrate, Inkjet-Printed Sensors for Health care, Advantage, Limitation and Future Scope of Inkjet Printing Technology for Printed Sensors	**8**	**Apply CO4**
Module-5: Wearable Biochemical and Gas Sensors		
Chemical Substances: Gas and Odor, Introduction, Human Odor-Based Sensors, Glucose, Introduction, Glucose Sensors, Noninvasive Glucose Monitoring Devices, GlucoWatch® G2 Biographer, GlucoTrackTM; Pulse oximeter, Portable Pulse Oximeters, wearable pulse oximeter; Wearable capnometer for monitoring of expired carbon dioxide. Textile based sensors	**8**	**Apply CO5**

Course Outcomes: After completing the course, the students will be able to	
23VDEP2253.1	To identify and understand the need for development of wearable devices and its influence on various sectors.
23VDEP2253.2	To understand various wearable inertial sensors for biomedical applications
23VDEP2253.3	To comprehend the design and development of various wearable technologies for use in healthcare applications
23VDEP2253.4	To realize the role of wearable locomotive sensors as assistive devices for tracking and navigation.
23VDEP2253.5	To Design and develop various wearable devices for detection of biochemical parameters.

Reference Books

1. Edward Sazonov, Michael R Neuman, "Wearable Sensors: Fundamentals, Implementation and Applications" Elsevier, 2nd Edition 2020.
2. "Seamless Healthcare Monitoring", Toshiyo Tamura and Wenxi Chen, Springer 2018.
3. "Wearable and Autonomous Biomedical Devices and Systems for Smart Environment", by Aimé Lay-Ekuakille and Subhas Chandra Mukhopadhyay, Springer 2010.
4. Subhas C. Mukhopadhyay, "Wearable Electronics Sensors-For Safe and Healthy Living", Springer International Publishing, 2015.
5. "Environmental, Chemical and Medical Sensors", by Shantanu Bhattacharya, A K Agarwal, Nripen Chanda, Ashok Pandey and Ashis Kumar Sen, Springer Nature Singapore Pte Ltd. 2018.

Dept. of Electronics and Communication Engineering
M. Tech (VLSI Design and Embedded Systems)
Choice Based Credit System (CBCS and Outcome Based Education (OBE)
Semester: II

Course Name: Project Management and Finance		**Course Code: 23VDE226**
L: T: P: J:	**3: 0: 0: 0**	**CIE Marks: 50**
Credits:	**3**	**SEE Marks: 50**
Hours/Week (Total):	**3 (40)**	**SEE Duration: 03 Hours**

Pre-Requisites: Basics of management and Management functions

Course Learning Objectives: The students will be able to

1	Understand Project and its classification
2	Understand Project identification and Selection
3	To design project using various tools
4	Understand the basic concepts of financial management and financial system.
5	Understand the sources of financing and make investment decisions.

Module-1: Introduction to Project Management	**No. of Hours**	**Blooms Cognitive Levels**
A Project. Search for a Business idea: Introduction, Choosing an Idea, Selection of product, The Adoption process, Product Innovation, Product Planning and Development Strategy, Product Planning and Development Process. Concepts of Projects and Classification: Introduction, Meaning of Projects, Characteristics of a Project, Project Levels, Project Classification, Aspects of a Project.	**08**	**Understand CO1**
Module-2: Project Cycle		
The project Cycle, Features and Phases of Project management, Project Management Processes. Project Identification: Feasibility Report, Project Feasibility Analysis. Project Formulation: Meaning, Steps in Project formulation, Sequential Stages of Project Formulation, Project Evaluation.	**08**	**Understand CO2**
Module-3: Project Design and Network Analysis		
Project Design and Network Analysis: Introduction, Importance of Network Analysis, Origin of PERT and CPM, Network, Network Techniques, Need for Network Techniques, Steps in PERT, CPM, Advantages, Limitations and Differences. Project design software tools.	**08**	**Apply CO3**
Module-4: Introduction to Financial Management		
Meaning and objectives of Financial Management, changing role of financemanagers. Interface of Financial Management with other functional areas. Indian Financial System: Financial markets, Financial Instruments, Financial institutions and financial services. Emerging issues in Financial Management: Risk Management, Behavioral Finance, Financial Engineering, Derivatives (Theory).	**08**	**Analyze CO4**
Module-5: Sources of Financing and Investment Decisions		
Shares, Debentures, Term loans, Lease financing, Hybrid financing, Venture Capital, Angel investing and private equity, Warrants and convertibles (Theory Only). Capital budgeting process, Investment evaluation techniques – Net present value, Internal rate of return, modified internal rate of return, Profitability index, Payback period, discounted payback period, accounting rate of return problem, Risk analysis in capital budgeting	**08**	**Understand CO5**

Course Outcomes: After completing the course, the students will be able to	
23VDE226.1	Define the Project and its classification
23VDE226.2	Explain steps in Project identification and Selection
23VDE226.3	Design projects using various tools network tools
23VDE226.4	Explain the basic concepts of financial management and financial system.
23VDE226.5	Explain the sources of financing and make investment decisions.

Reference Books

1. Essentials of Management: An International, Innovation and Leadership perspectiveby Harold Koontz, Heinz Weihrich McGraw Hill Education, 10th Edition 2016. ISBN- 978-93-392-2286-4.
2. Avery N. Goldstein, Patent Law for Scientists and Engineers, Taylor & Francis /1st Edition/ 2005
3. Dynamics of Entrepreneurial Development and Management by Vasant Desai. HPH 2007, ISBN: 978-81-8488-801-2.
4. Professional Programme Intellectual Property Rights, Law and Practice, The Instituteof Company Secretaries of India, Statutory Body Under an Act of Parliament, September 2013. Study Material (For the topic Intellectual Property under module 4 and 5)
5. Ganguli Prabuddha, Intellectual Property Rights--Unleashing the Knowledge Economy, Tata McGrawHill (2001).
6. Financial Management by Prasanna Chandra, TMH 9/e.
7. Financial Management: A Strategic Perspective Nikhil Chandra Shil & Bhagaban Das, Sage Publications 1/e, 2016.
8. Financial Management by Khan M. Y.& Jain P. K, TMH 7/e.

Marks Distribution for Assessment:

PCC	CIA	SEA	CIA (50)			SEA **Conduction: 100 M** **Reduced to: 50 M**
				I	II	
Conduction	50	50	Written Test	50	50	Five questions with each of 20 marks (with internal choice). Student should answer one full question from each module
				Average of two tests – 25 Marks		
			Assignment	15		
			AAT	10		
			Total – 50 marks			**Total – 50 marks**

i) CIA: 50%

IA Test: 2 IA tests - Each of 50 Marks	Average of 2 tests – scaled down to 25 M
Assignment – Two assignments – one for 10 marks and another for 5 marks	15 Marks
Additional Assessment Tools (AAT) – Oral /Online Quizzes, Presentations, Group discussions, Case studies, Term Paper, Open ended experiments, Mini industrial/social/rural Projects, Two-minute video on latest topic, Short MOOC courses, Practical Orientation on Design thinking, creativity & Innovation, Participatory & Industry integrated learning, Practical activities, Problem solving exercises, Participation in seminars/academic events/symposia and any other activity	10 Marks
Total	**50 Marks**

ii) SEA : 50%

Theory Exam	5 questions to answer each of 20 Marks 2 questions from each module with internal choice Student should answer one full question from each module	20 M x 5 = **100 M** **reduced to 50 M**
	Total	**50 Marks**

M. Tech. (VLSI Design & Embedded System)
Choice Based Credit System (CBCS and Outcome Based Education (OBE)

Semester: 3

Course Name: CMOS RF Circuits Design **Course Code: 23VDE231**

L: T: P: J	**3:0:0:0**	**CIA Marks: 50**
Credits:	**3**	**SEA Marks: 50**
Hours/Week (Total)	**3**	**SEA Duration:** 03 Hours

Course Learning Objectives: The students will be able to

1	Learn basic concepts in RF and microwave design emphasizing the effects of nonlinearity and noise.
2	Appreciate communication system, multiple access techniques and wireless standards necessary for RF circuit design.
3	Deal with transceiver architecture, various receiver and transmitter designs, their merits and demerits.
4	Understand the design of RF building blocks such as Low Noise Amplifiers, Mixers.
5	Understand the working principal of Oscillators, VCOs, Frequency Synthesizers and PLLs

Module 1: Introduction to RF Design, Wireless Technology and Basic Concepts	**No. of Hours**	**Blooms cognitive Levels**
A wireless world, RF design is challenging, The big picture. General considerations, Units in RF Design, Time Variance, Nonlinearity, Effects of Nonlinearity, Harmonic Distortion, Gain Compression, Cross Modulation, Intermodulation, Cascaded Nonlinear Stages, AM/PM Conversion, Noise, Noise as a Random Process, Noise Spectrum, Effect of Transfer Function on Noise, Device Noise, Representation of Noise in Circuits.	**8**	**Apply CO1**
Module-2 Passive Impedance Transformation and Communication Concepts		
Passive Impedance Transformation: Quality Factor, Series-to-Parallel Conversion, Basic Matching Networks, Loss in Matching Networks. **Communication Concepts:** General concepts, analog modulation, digital modulation, spectral re-growth. Mobile RF communications, Multiple access techniques, Wireless standards Specifications only.	**8**	**Apply CO2**
Module-3 Transceiver Architecture		
Receivers: General Considerations, Receiver Architectures, Basic Heterodyne Receivers, Modern Heterodyne Receivers, Direct-Conversion Receivers, Image-Reject Receivers. **Transmitters**: Transmitter Architectures, General Considerations, Direct-Conversion, Transmitters, Modern Direct-Conversion Transmitters, Heterodyne Transmitters.	**8**	**Apply CO3**
Module-4 Low Noise Amplifiers and Mixers		
Low Noise Amplifiers: General considerations, Problem of input matching, LNA topologies: common-source stage with inductive load, common-source stage with resistive feedback, Common Gate stage (only upto Input impedance). **Mixers:** General considerations, Performance parameters, Mixer Noise Figures, Single balanced and Double balanced mixers, Passive download Mixers, Gain, LO self-mixing, Noise, Input Impedance, Current driven passive mixers.	**8**	**Apply CO4**
Module-5 VCO, PLLs and Power Amplifiers		
VCOs: Voltage-Controlled Oscillators (VCOs), Tuning Range Limitations, Effect of Varactor Q, Phase Noise, Basic Concepts, Effect of Phase Noise, Design Procedure, Low-Noise VCOs, LO Interface, Quadrature Oscillators, Basic Concepts **Phase-Locked Loops (PLLs):** Basic Concepts, Phase Detector, TYPE-I	**8**	**Apply CO5**

Synthesizers, General Considerations, Basic Integer-*N* Synthesizer **Power Amplifiers:** General Considerations, Classification of Power Amplifiers, Class A Power Amplifiers, Class B Power Amplifiers, Class AB Power Amplifiers, Class C Power Amplifiers		

Course Outcomes: After completing the course, the students will be able to	
23VDE231.1	Analyze the effect of nonlinearity and noise in RF and microwave design.
23VDE231.2	Understand communication system, multiple access techniques and wireless standards necessary for RF circuit design.
23VDE231.3	Describe various receivers and transmitter topologies with their merits and drawbacks.
23VDE231.4	Design Mixers and Low-Noise Amplifiers with minimum number of off-chip components.
23VDE231.5	Exemplify the approaches taken in the design of VCOs, PLLs, Frequency synthesizers and Power amplifiers.
23VDE231.6	Illustrate how the system requirements define the parameters of the circuits and the impact on the performance.

Reference Books

1. RF Microelectronics, B. Razavi, PHI, second edition.
2. CMOS Circuit Design, layout and Simulation, R. Jacob Baker, H.W. Li, D.E. Boyce, PHI 1998

PCC	**CIA**	**SEA**	**CIA (50)**			**SEA** **Conduction: 100 M** **Reduced to: 50 M**
				I	II	
Conduction	50	50	Written Test	50	50	Five questions with each of 20 marks (with internal choice). Student should answer one full question from each module
				Average of two tests – 25 Marks		
			Assignment	15		
			AAT	10		
			Total – 50 marks			**Total – 50 marks**

i) CIA: 50%

IA Test: 2 IA tests - Each of 50 Marks	Average of 2 tests – scaled down to 25 M
Assignment – Two assignments – one for 10 marks and another for 5 marks	15 Marks
Additional Assessment Tools (AAT) – Oral /Online Quizzes, Presentations, Group discussions, Case studies, Term Paper, Open ended experiments, Mini industrial/social/rural Projects, Two-minute video on latest topic, Short MOOC courses, Practical Orientation on Design thinking, creativity & Innovation, Participatory & Industry integrated learning, Practical activities, Problem solving exercises, Participation in seminars/academic events/symposia and any other activity	10 Marks
Total	**50 Marks**

ii) SEA: 50%

Theory Exam	5 questions to answer each of 20 Marks 2 questions from each module with internal choice Student should answer one full question from each module	20 M x 5 = **100 M** **reduced to 50 M**
	Total	**50 Marks**

M. Tech. (VLSI Design & Embedded System)
Choice Based Credit System (CBCS and Outcome Based Education (OBE)

Semester: III

Course Name: CAD for Digital Systems		**Course Code: 23VDE232**
L: T: P: J	**3:0:0:0**	**CIA Marks: 50**
Credits:	**3**	**SEA Marks: 50**
Hours/Week (Total)	**3**	**SEA Duration:** 03 Hours

Pre-Requisites: Digital electronics

Course Learning Objectives: The students will be able to

1	To use the algorithms of Graph theory for optimization and satisfiability.
2	To be able to differentiate between P, NP and NPC problems
3	To use graph theory in physical design.
4	To understand the time and space complexities.
5	To learn various optimization methods.
6	To understand different techniques for placement and routing.

Module-1: Introduction to Design Methodologies and Graph theory	**No. of Hours**	**Blooms cognitive Levels**
The VLSI Design Problem, The Design Domains, Design Actions, Design methods and Technologies. VLSI Design Automation tools: Algorithmic and System Design, Structural and Logic Design, Transistor-level Design, Layout Design, Verification Methods, Design Management Tools. Algorithmic graph theory and computational complexity: Terminology, Data Structures for the Representation of Graphs, Computational Complexity, Examples of Graph Algorithms. Tractable and intractable problems: Decision Problems, Complexity Classes, NP-completeness and NP-hardness, Consequences.	**8**	**Understand CO1**
Module-2: Combinatorial optimization and Layout compaction		
General purpose methods for combinational optimization: Backtracking and Branch-and-bound, Dynamic Programming, Integer Linear Programming, Local Search, Simulated Annealing, Tabu Search, Genetic Algorithms, A Few Final Remarks on General-purpose Methods. Layout compaction: Design Rules, Symbolic Layout, Problem Formulation, Algorithms for Constraint-graph Compaction, Other Issues.	**8**	**Apply CO2**
Module-3: Physical Design		
Placement and partitioning: Circuit Representation, Wire-length Estimation, Types of Placement Problem, Placement Algorithm, Partitioning. Floor planning: Floorplanning Concepts, Shape Functions and Floorplan Sizing. Routing: Types of Local Routing Problems, Area Routing, Channel Routing, Introduction to Global Routing, Algorithms for Global Routing. Machine Learning in Physical Verification, Mask Synthesis, and Physical Design (Reference- 1)	**8**	**Apply CO3**
Module-4: Logic Synthesis and Simulation – I		
Logic Synthesis and Verification: Introduction to Combinational Logic Synthesis, Binary-decision Diagrams, Two-level Logic Synthesis. Simulation: General Remarks on VLSI Simulation, Gate-level Modelling and Simulation	**8**	**Apply CO4**
Module-5: Logic Synthesis – II		
High level Logic synthesis: Hardware Models for High Level Synthesis, Internal Representation of the Input Algorithm, Allocation, Assignment and Scheduling, Some Scheduling Algorithm, Some Aspects of the	**8**	**Understand CO5**

minimization – completely specified and incompletely specified, Compatibility classes, State encoding, Structural representation of sequential circuits, Retiming, Extension		

Course Outcomes: After completing the course, the students will be able to	
23VDE232.1	Demonstrate knowledge and understanding of fundamental concepts in VLSI design using CAD.
23VDE232.2	Solve graph theoretical problems.
23VDE232.3	Demonstrate knowledge of computational and optimization algorithms applicable to solving CAD related problems.
23VDE232.4	Establish comprehensive understanding of the various phases of CAD for digital electronic systems, from digital logic simulation to physical design
23VDE232.5	Demonstrate the relationship between optimization during synthesis and verification with satisfiability and formal verification
23VDE232.6	Demonstrate knowledge of computational and optimization tools applicable to solving CAD related problems.

Reference Books

1. **Algorithms for VLSI Design Automation -** S H Gerez, Wiley, 2nd Edition.
2. **Synthesis and Optimization of Digital circuits –**
3. **Machine Learning in VLSI Computer-Aided Design - Elfadel**, Ibrahim (Abe) M., **Boning**, Duane S., **Li**, Xin (Eds.), Springer, 2019
4. **Advanced Logic Synthesis - Reis**, André Inácio, **Drechsler**, Rolf (Eds.), Springer, 2018

PCC	**CIA**	**SEA**	**CIA (50)**			**SEA Conduction: 100 M Reduced to: 50 M**
				I	II	
Conduction	50	50	Written Test	50	50	Five questions with each of 20 marks (with internal choice). Student should answer one full question from each module
				Average of two tests – 25 Marks		
			Assignment	15		
			AAT	10		
			Total – 50 marks			**Total – 50 marks**

i) CIA: 50%

IA Test: 2 IA tests - Each of 50 Marks	Average of 2 tests – scaled down to 25 M
Assignment – Two assignments – one for 10 marks and another for 5 marks	15 Marks
Additional Assessment Tools (AAT) – Oral /Online Quizzes, Presentations, Group discussions, Case studies, Term Paper, Open ended experiments, Mini industrial/social/rural Projects, Two-minute video on latest topic, Short MOOC courses, Practical Orientation on Design thinking, creativity & Innovation, Participatory & Industry integrated learning, Practical activities, Problem solving exercises, Participation in seminars/academic events/symposia and any other activity	10 Marks
Total	**50 Marks**

ii) SEA: 50%

Theory Exam	5 questions to answer each of 20 Marks 2 questions from each module with internal choice Student should answer one full question from each module	20 M x 5 = **100 M reduced to 50 M**

M. Tech. (VLSI Design & Embedded System)
Choice Based Credit System (CBCS and Outcome Based Education (OBE)

Semester: 3

Course Name: VLSI Design Signal Processing **Course Code: 23VDEP2331**

L: T: P: J	**3:0:0:0**	**CIA Marks: 50**
Credits:	**3**	**SEA Marks: 50**
Hours/Week (Total)	**3**	**SEA Duration:** 03 Hours

Course Learning Objectives: The students will be able to

1	Learn several high-level architectural transformations that can be used to design families of architectures for a given algorithm.
2	Deal with high-level algorithm transformations such as strength reduction, look-ahead and relaxed look-ahead

Module 1	**No. of Hours**	**Blooms cognitive Levels**
Introduction to DSP Systems: Typical DSP Algorithms, DSP Application Demands and Scaled CMOS Technologies, Representations of DSP Algorithms. **Iteration Bounds:** Data flow graph Representations, loop bound and Iteration bound. Algorithms for Computing Iteration Bound, Iteration Bound of multi rate data flow graphs.	**8**	**Apply CO1**
Module-2		
Pipelining and Parallel Processing: pipelining of FIR Digital Filters, parallel processing, Pipelining and parallel processing for low power. **Retiming:** Definition and Properties, Solving Systems of Inequalities, Retiming Techniques.	**8**	**Apply CO2**
Module-3		
Unfolding: An Algorithm for Unfolding, Properties of Unfolding, Critical path, Unfolding and Retiming, Application of Unfolding. **Folding:** Folding Transformation, Register Minimization Techniques, Register Minimization in Folded Architectures, Folding of Multirate Systems.	**8**	**Apply CO3**
Module-4		
Systolic Architecture Design: systolic array design Methodology, FIR systolic array, Selection of Scheduling Vector, Matrix-Matrix Multiplication and 2D systolic Array Design, Systolic Design for space representation containing Delays. **Fast convolution**: Cook-Toom Algorithm, Winograd Algorithm, Iterated convolution, cyclic convolution Design of fast convolution Algorithm by Inspection.	**8**	**Apply CO4**
Module-5		
Algorithmic Strength Reduction in Filters and Transforms: Parallel FIR Filters, DCT and Inverse DCT, Parallel Architecture for Rank Order Filters **Pipelined and Parallel Recursive and Adaptive Filter**: Pipeline Interleaving in Digital Filter, first order IIR digital Filter, Higher order IIR digital Filter, parallel processing for IIR filter, Combined pipelining and parallel processing for IIR Filter, Low power IIR Filter Design Using Pipelining and parallel processing, pipelined adaptive digital filter	**8**	**Apply CO5**

Course Outcomes: After completing the course, the students will be able to	
23VDEP2331.1	Illustrate the use of various DSP algorithms and addresses their representation using block diagrams, signal flow graphs and data-flow graphs
23VDEP2331.2	Use pipelining and parallel processing in design of high-speed /low power applications
23VDEP2331.3	Apply unfolding in the design of parallel architecture
23VDEP2331.4	Evaluate the use of look-ahead techniques in parallel and pipelined IIR Digital filters
23VDEP2331.5	Develop an algorithm or architecture or circuit design for DSP applications

Reference Books

1. VLSI Digital Signal Processing systems, Design and implementation, Keshab K.Parthi, Wiley 1999 .
2. Analog VLSI Signal and Information Processing, Mohammed Isamail and Terri Fiez, Mc Graw-Hill,1994
3. VLSI and Modern Signal Processing, S.Y. Kung, H.J. White House, T. Kailath, Prentice Hall, 1994
4. Design of Analog - Digital VLSI Circuits for Telecommunication and Signal Processing, Jose E. France, Yannis Tsividis, Prentice Hall, 1994
5. DSP Integrated Circuits, Lars Wanhammar, Academic Press Series in Engineering, 1st Edition.

PCC	CIA	SEA	CIA (50)			SEA **Conduction: 100 M** **Reduced to: 50 M**
				I	II	
Conduction	50	50	Written Test	50	50	Five questions with each of 20 marks (with internal choice). Student should answer one full question from each module
				Average of two tests – 25 Marks		
			Assignment	15		
			AAT	10		
			Total – 50 marks			**Total – 50 marks**

i) CIA: 50%

IA Test: 2 IA tests - Each of 50 Marks	Average of 2 tests – scaled down to 25 M
Assignment – Two assignments – one for 10 marks and another for 5 marks	15 Marks
Additional Assessment Tools (AAT) – Oral /Online Quizzes, Presentations, Group discussions, Case studies, Term Paper, Open ended experiments, Mini industrial/social/rural Projects, Two-minute video on latest topic, Short MOOC courses, Practical Orientation on Design thinking, creativity & Innovation, Participatory & Industry integrated learning, Practical activities, Problem solving exercises, Participation in seminars/academic events/symposia and any other activity	10 Marks
Total	**50 Marks**

ii) SEA: 50%

Theory Exam	5 questions to answer each of 20 Marks 2 questions from each module with internal choice Student should answer one full question from each module	20 M x 5 = **100 M reduced to 50 M**
	Total	**50 Marks**

Dept. of Electronics and Communication Engineering
Choice Based Credit System (CBCS and Outcome Based Education (OBE)

Semester: III

Course Name: Machine Learning using Python		**Course Code: 23VDPE2332**
L: T: P: J	**3 :0 :0 :0**	**CIA Marks:** 50
Credits:	**3**	**SEA Marks:** 50
Hours/Week (Total)	**3**	**SEA Duration:** 03 Hours

Pre-Requisites: Programming knowledge

Course Learning Objectives: The students will be able to

1	Introduce basic concepts of Machine Learning and Python
2	Apply the knowledge of data preprocessing and regression and solve problems
3	Apply statistical knowledge to understand and interpret the relevance of the algorithm outcome
4	Apply classification algorithms and supervised learning
5	Apply unsupervised learning and preprocessing techniques

Module-1: Introduction	**No. of Hours**	**Blooms Cognitive Levels**
Overview of Machine Learning, building intelligent machines to transform data into knowledge, three different types of machine learning, An introduction to thebasic terminology and notations, A roadmap for building machine learning systems Python libraries suitable for Machine Learning: Numerical Analysis and Data Exploration with NumPy Arrays, and Data	**8**	**Apply CO1**
Module-2: Data preprocessing and Linear Regression		
Introduction to Machine learning, building a machine learning model, Data preprocessing, data exploration, outlier treatment, imputation. Correlation analysis, Simple Linear Regression, Multiple Linear Regression. Problem solving in Python	**8**	**Apply CO2**
Module-3: Statistics for Machine Learning		
Introduction, Mean, Median and Mode, Standard Deviation, Percentiles, scatterplot, types of data, measures of centers, measures of dispersion. Problem solving in Python	**8**	**Apply CO3**
Module-4: Classification models		
Introduction to Classification models, Logistic Regression, K-nearest neighbors (KNN), and Linear Discriminant Analysis (LDA). Classification problems on prediction using Python	**8**	**Apply CO4**
Module-5: Decision trees and SVM		
Simple decision trees, simple classification tree. Ensemble techniques-Bagging, Random Forest, Boosting Support Vector Machines – Introduction, Support Vector classifiers,Creating SVM model in Python	**8**	**Apply CO5**

Course Outcomes: After completing the course, the students will be able to	
23VDPE2332.1	Introduce basic concepts of Machine Learning and Python
23VDPE2332.2	Apply the knowledge of data preprocessing and regression and solve problems
23VDPE2332.3	Apply statistical knowledge to understand and interpret the relevance of the algorithm outcome
23VDPE2332.4	Apply classification algorithms and supervised learning
23VDPE2332.5	Apply unsupervised learning and preprocessing techniques
23VDPE2332.6	Able to apply the knowledge of machine learning to real-life scenarios.

Reference Books

1. Chris Albon, Machine Learning with Python Cookbook, O'Reilly, 2018.
2. E.Alpaydin, Introduction to Machine Learning, Prentice-Hall of India, 2010

PCC	CIA	SEA	CIA (50)			SEA Conduction: 100 M Reduced to: 50 M
				I	II	
Conduction	50	50	Written Test	50	50	Five questions with each of 20 marks (with internal choice). Student should answer one full question from each module
				Average of two tests – 25 Marks		
			Assignment	15		
			AAT	10		
			Total – 50 marks			**Total – 50 marks**

i) CIA: 50%

IA Test: 2 IA tests - Each of 50 Marks	Average of 2 tests – scaled down to 25 M
Assignment – Two assignments – one for 10 marks and another for 5 marks	15 Marks
Additional Assessment Tools (AAT) – Oral /Online Quizzes, Presentations, Group discussions, Case studies, Term Paper, Open ended experiments, Mini industrial/social/rural Projects, Two-minute video on latest topic, Short MOOC courses, Practical Orientation on Design thinking, creativity & Innovation, Participatory & Industry integrated learning, Practical activities, Problem solving exercises, Participation in seminars/academic events/symposia and any other activity	10 Marks
Total	**50 Marks**

ii) SEA: 50%

Theory Exam	5 questions to answer each of 20 Marks 2 questions from each module with internal choice Student should answer one full question from each module	20 M x 5 = **100 M reduced to 50 M**
	Total	**50 Marks**

M. Tech. (VLSI Design & Embedded System)
Choice Based Credit System (CBCS and Outcome Based Education (OBE)

Semester: III

Course Name: Synthesis and Optimization of Digital Circuits **Course Code: 23VDEP2333**

L: T: P: J	**3:0:0:0**	**CIA Marks: 50**
Credits:	**3**	**SEA Marks: 50**
Hours/Week (Total)	**3**	**SEA Duration:** 03 Hours

Course Learning Objectives: The students will be able to

1	Understand the need for optimization and dimensions of optimization for digital circuits.
2	Learn basic optimization techniques used in circuits design.
3	Get the knowledge of advanced tools and techniques in digital systems design like Hardware Modelling and Compilation Techniques.
4	Apply Logic-Level synthesis and optimization techniques for combinational and sequential circuits.
5	Infer concept of scheduling and resource binding for optimization

Module 1: Introduction to Synthesis, Optimization & Hardware modelling	**No. of Hours**	**Blooms cognitive Levels**
Introduction to Synthesis and optimization: Design of Microelectronics circuits, Computer aided Synthesis and Optimization. **Hardware Modelling**: Introduction, Hardware Modelling Languages, Distinctive Features of Hardware Languages, Structural Hardware Languages, Behavioural Hardware Languages, HDLs Used for Synthesis, Abstract Models, Compilation and Behavioural Optimization **Architectural Synthesis and Optimization:** Fundamental Architectural Synthesis problems, Area and Performance Estimation, Strategies for Architectural Optimization	**8**	**Apply CO1**
Module-2 Graph theory for CAD for VLSI		
Graphs, Combinatorial Optimization, Graph Optimization problems and Algorithms, Boolean Algebra and Applications.	**8**	**Apply CO2**
Module-3 Two level and Multiple Level Combinational Logic Optimization		
Two level Combinational Logic Optimization: Introduction, Logic Optimizations, Operations on Two level Logic Covers **Multiple Level Combinational Logic Optimization**: Introduction, Models and Transformations for Combinational Networks, The Algebraic Model, The Boolean Model	**8**	**Apply CO3**
Module-4 Sequential Logic Optimization		
Introduction, Sequential Logic Optimization using State based Models, Sequential Logic Optimization using Network Models, Implicit FSM Traversal Methods, Testability Considerations for Synchronous Circuits	**8**	**Apply CO4**
Module-5 Scheduling Algorithms and Resource Sharing and Binding		
Scheduling Algorithms: Introduction, A Model for Scheduling problems, Scheduling with Resource Constraints, scheduling without Resource Constraints, Scheduling Algorithms for Extended Sequencing Models, Scheduling Pipelined Circuits. **Resource Sharing and Binding:** Sharing and Binding for Resource dominated circuits, Sharing and Binding for General Circuits, Concurrent Binding and Scheduling, Resource sharing and Binding for Non – Scheduled Sequencing Graphs.	**8**	**Apply CO5**

Course Outcomes: After completing the course, the students will be able to	
23VDEP2333.1	Understand the process of synthesis and optimization in a top-down approach for digital circuit models using HDLs and Architecture.
23VDEP2333.2	Understand the terminologies of graph theory and its algorithms to optimize a Boolean equation
23VDEP2333.3	Apply different two level and multilevel optimization algorithms for combinational circuits.
23VDEP2333.4	Apply the different sequential circuit optimization methods using state models and network models.
23VDEP2333.5	Apply different scheduling algorithms with resource binding and without resource binding for pipelined sequential circuits and extended sequencing models.

Reference Books

1. Synthesis and Optimization of Digital Circuits, Giovanni De Micheli, Tata McGraw-Hill, 2003
2. Automatic Logic synthesis Techniques for Digital Systems, Edwars M. D, Macmillan New Electronic Series, 1992

<table>
<tr><th rowspan="2">PCC</th><th rowspan="2">CIA</th><th rowspan="2">SEA</th><th colspan="3">CIA (50)</th><th rowspan="2">SEA
Conduction: 100 M
Reduced to: 50 M</th></tr>
<tr><th></th><th>I</th><th>II</th></tr>
<tr><td rowspan="5">Conduction</td><td rowspan="5">50</td><td rowspan="5">50</td><td rowspan="2">Written Test</td><td>50</td><td>50</td><td rowspan="4">Five questions with each of 20 marks (with internal choice). Student should answer one full question from each module</td></tr>
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<tr><td>Assignment</td><td colspan="2">15</td></tr>
<tr><td>AAT</td><td colspan="2">10</td></tr>
<tr><td colspan="3">Total – 50 marks</td><td>Total – 50 marks</td></tr>
</table>

i) CIA: 50%

IA Test: 2 IA tests - Each of 50 Marks	Average of 2 tests – scaled down to 25 M
Assignment – Two assignments – one for 10 marks and another for 5 marks	15 Marks
Additional Assessment Tools (AAT) – Oral /Online Quizzes, Presentations, Group discussions, Case studies, Term Paper, Open ended experiments, Mini industrial/social/rural Projects, Two-minute video on latest topic, Short MOOC courses, Practical Orientation on Design thinking, creativity & Innovation, Participatory & Industry integrated learning, Practical activities, Problem solving exercises, Participation in seminars/academic events/symposia and any other activity	10 Marks
Total	**50 Marks**

ii) SEA: 50%

Theory Exam	5 questions to answer each of 20 Marks 2 questions from each module with internal choice Student should answer one full question from each module	20 M x 5 = **100 M** **reduced to 50 M**
	Total	**50 Marks**